University of Alberta

CURRENT-BASED TEST IN DEEP SUB-MICRON ENVIRONMENT

by

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People like us, who believe in physics, know that
the distinction between past, present, and future
is only a stubbornly persistent illusion.

— Albert Einstein, 1879-1955

Abstract

Integrated circuit test strategies and their implementations have been driven by the trade-off between a test cost and its effectiveness. Technology trends in the semiconductor industry enabled manufacturing of a transistor device with a dramatically reduced feature size, which provided a foundation for the exponential increase in densities, complexities, and frequencies of integrated circuits. These trends, however, presented more complex test environments which resulted in degraded quality of the conventional specification or fault-model-based test methods and a significantly higher manufacturing test cost.

Current-based test has been an important failure analysis and characterization tool, indispensable for test quality improvement, test cost reduction, and burn-in elimination. Highly integrated deep sub-micron technology processes, characterized by the exponential increase of leakage currents as well as reduced control over process variations, render existing current-based test methods less effective with constantly declining capabilities. Most notable challenges arise from the difficulties to access deeply embedded circuits, perform accurate and fast current measurements, and process the signals so that useful information could be extracted and interpreted for the test purpose.

This thesis investigates the application of the current-based test methodology for digital and analog circuits in a deep sub-micron environment. A built-in current monitoring solution has been identified as a strong opportunity to address the challenges by enabling easier access to an embedded core. A topology of the versatile CMOS current sensing device is proposed as a built-in self-test monitor for conventional digital/analog I_{DDQ} power supply current test. A novel sensor topology

is successfully employed in a current monitoring testing scheme. The presented sensor is a scalable and practical embedded solution for high-frequency parametric I_{DDQ} test of standard CMOS integrated circuits.

A feasibility of a structural model-based method for testing analog integrated circuits has been explored. The proposed method is an extension of digital I_{DD} test to analog circuits. We investigated the detection rate based on the resistive open and short fault model within a MOSFET device. Input test signals are optimized for maximum detectability of introduced faults. The stimuli required for defect screening are DC signals which can be easily produced on-chip. This simple yet effective method is suitable for production testing, as a preliminary and complementary test of embedded analog circuits for early defect screening in highly integrated environments.

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Nomenclature

List of Acronyms

ABM	Analog Boundary Modules, page 29
AC	Alternating Current, page 10
ASIC	Application-Specific Integrated Circuit, page 27
ATAP	Analog Test Access Port, page 29
ATE	Automatic Test Equipment, page 3
ATPG	Automatic Test Pattern Generation, page 23
BICS	Built-In Current Sensor, page 67
BIST	Built-In Self-Test, page 29
BSC	Boundary Scan Cell, page 25
CAD	Computer-Aided Design, page 9
CM	Current Monitor, page 67
CMOS	Complementary Metal-Oxide Semiconductor, page 1
CR	Current Ratios, page 60
CUT	Circuit Under Test, page 77
CV	Current Voltage, page 56
DBT	Defect-Based Test, page 22
DC	Direct Current, page 10
DFT	Design For Testability, page 24
DIBL	Drain-Induced Barrier Lowering, page 48

DLFT	Die-Level Functional Test, page 14
DPS	Device Power Supply, page 75
DRAM	Dynamic Random-Access Memory, page 3
DSP	Digital Signal Processor, page 27
DUT	Device Under Test, page 69
ECR	Energy Consumption Ratio, page 39
EEPROM	Electrically-Erasable Programmable Read-Only Memory, page 19
EM	Electromigration, page 17
EOS	Electrical Over-Stress, page 18
ESD	Electrostatic Discharge, page 18
FET	Field-Effect Transistor, page 1
FN	Fowler-Nordheim tunneling, page 55
GIDL	Gate-Induced Drain Leakage, page 49
GOS	Gate-Oxide Short, page 21
HCI	Hot Carrier Injection, page 17
I/O	Input/Output, page 77
IEEE	Institute of Electrical and Electronics Engineers, page 28
IFA	Inductive Fault Analysis, page 33
ITRS	International Technology Roadmap for Semiconductors, page 139
LBIST	Logic Built-In Self-Test, page 30
LOCOS	LOCal Oxidation of Silicon, page 51
MAGFET	Magnetic Field-Effect Transistors, page 74
MBIST	Memory Built-In Self-Test, page 30
MDS	Minimum Detectable Signal, page 128
MOS	Metal-Oxide Semiconductor, page 1
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor, page 1

MP	Microprocessor, page 27
MR	Magnetoresistor, page 74
MT	Magnetotransistor, page 74
MTCMOS	Multi-Threshold CMOS, page 66
NMOS	N-type Metal-Oxide Semiconductor, page 32
PMOS	P-type Metal-Oxide Semiconductor, page 32
PMU	Precision Measurement Unit, page 75
PSD	Power Supply Degradation, page 117
QA	Quality Assurance, page 14
QTAG	Quality Test Action Group, page 76
RBB	Reverse Body Bias, page 58
RC	Resistive Capacitive, page 71
RCA	Ripple Carry Adder, page 123
RF	Radio Frequency, page 30
RF BIST	Radio Frequency Built-In Self-Test, page 30
SCE	Short Channel Effects, page 45
SoC	System-on-Chip, page 27
SRAM	Static Random-Access Memory, page 3
ST	Sensitivity Threshold, page 171
TBIC	Test Bus Interface Circuit, page 29
TCK	Test Clock, page 27
THD	Total Harmonic Distortion, page 115
TMS	Test Mode Select, page 27
VDSM	Very Deep Sub-Micron, page 58
VLSI	Very Large Scale of Integration, page 2
VTCMOS	Variable-Threshold CMOS, page 66

List of Symbols

ΔQ_B	Incremental depletion charge in the bulk, page 52
μ_0	Electron mobility, page 47
ϕ_s	Surface potential, page 52
A_i	Total area of the i^{th} p-n junction, page 46
C_F	Sidewall capacitance, page 53
C_T	Overall gate capacitance, page 53
C_c	Compensation capacitor, page 107
C_{dm}	Capacitance of the depletion layer, page 47
C_{ox}	Gate oxide capacitance, page 47
eV	Electronvolt, page 57
g_{m_X}	Transconductance of transistor M_X, page 105
g_{mb_X}	Body transconductance of transistor M_X, page 100
I_{bias}	Output stage biasing current, page 114
I_{DC}	Input stage biasing current, page 99
I_{DDQ}	Static/quiescent power supply current, page 32
I_{DDT}	Dynamic/transient power supply current, page 34
I_{DD}	Power supply current, page 32
I_D	Drain current, page 44
I_{gc}	Gate-to-channel tunneling current, page 54
I_{gdo}	Gate-to-drain tunneling current, page 54
I_{gso}	Gate-to-source tunneling current, page 54
I_{OFF}	Off-state leakage current, page 44
I_{RB}	Reverse bias p-n junction leakage current, page 46
J_s	Reverse saturation current density of the p-n junction, page 46

k	Boltzmann's constant, page 47
L	Length of MOSFET transistor, page 47
L_{eff}	Effective channel length of MOSFET device, page 48
M_X	Conventional name of MOSFET device, page 97
n	Subthreshold swing coefficient, page 47
N_{sub}	Substrate doping, page 52
q	Electron charge, page 47
Q_B	Depletion charge in the bulk, page 52
R_F	Source follower resistor, page 97
R_L	Load resistance, page 106
r_{ox}	Incremental output resistance of transistor M_X, page 100
R_{on}	Resistance of the forward conducting MOSFET, page 72
R_S	Current sensing resistor, page 98
S_{subth}	Subthreshold slope, page 47
T	Absolute temperature, page 47
t_{ox}	Gate oxide thickness, page 47
V_{DD}	Power supply voltage, page 35
V_{DG}	Drain-to-gate voltage, page 49
V_D	Drain voltage, page 44
V_{fb}	Flat-band voltage, page 52
V_{GS}	Gate-to-source voltage, page 44
V_G	Gate voltage, page 48
V_{NCE}	Narrow channel width effect voltage, page 52
V_{SB}	Source-to-substrate voltage, page 48
V_S	Source voltage, page 97
V_{TH}	Threshold voltage, page 44

V_t	Thermal voltage, page 47
W	Width of MOSFET transistor, page 47
W_{dm}	Maximum depletion layer width, page 47
W_{eff}	Effective channel width of MOSFET device, page 52
$x_{d.max}$	Maximum vertical depletion width, page 52
Z_{in}	Input impedance, page 108

List of Terms

active fault	Fault which causes an incorrect behavior of the circuit only when a specific state occurs in some other part of the circuit, page 37
at-speed test	Test performed at a nominal operational frequency of a circuit under test, page 3
catastrophic short	Short with zero resistance between its nodes, page 21
dangling bond	Dangling bond occurs when an atom is missing a neighbor to which it would be able to bind, page 57
defect	Physical imperfection in the implementation of the IC circuit, page 15
defect level	Percentage of defective chips that escape the testing process, page 9
defect-based test	Structural test method which targets physical defects through defect-oriented fault models, page 22
defect-oriented fault	Fault modeled at the physical/transistor level, page 16
delay fault	Fault which causes a combinational delay of the circuit to exceed the clock period, page 16
direct tunneling	Tunneling in MOS devices with ultra-thin oxide during which electrons from the conduction band in semiconductor are transferred across the oxide directly into the conduction band of metal, page 55
electromigration	Transport of material caused by the gradual movement of the ions in a conductor due to the high density of electrical current, page 17
equivalent faults	Faults which transform a circuit to have identical output function, page 22
failure	Mechanism which causes the occurrence of defects, page 16
fault	Representation of the class of defects by using a given fault model, page 16
fault collapsing	Partitioning all faults into the sets of equivalent ones, page 22

fault coverage	Ratio of the number of detected faults over total number of all possible faults, page 23
fault efficiency	Ratio of the number of detected faults over total number of all testable faults, page 23
floating gate	Gate of transistor disconnected from the rest of the circuit, page 21
FN tunneling	Tunneling of electrons from the semiconductor conduction band into the oxide conduction band through the potential barrier at the semiconductor-oxide interface, page 55
Hall effect	Potential difference on opposite sides of a thin sheet of conducting or semiconducting material through which an electric current is flowing, created by a magnetic field applied perpendicular to the conducting material, page 74
heterogenous system	System containing broad spectrum of different types of circuits and devices (*e.g.*, analog, RF, digital,...), page 3
impact ionization	Generation of electron-hole pairs in semiconductor when high kinetic energy electrons collide with atoms in a lattice, page 57
inductive fault analysis	Systematic method for determining the realistic faults likely to occur in a VLSI circuit, page 33
infant mortality	Failure rate during the early stage of IC operation, page 34
integrated circuit	Electronic circuit with a number of devices fabricated and interconnected on a single semiconductor material, page 2
Moore's Law	Empirical observation stating that the number of transistors per square inch on integrated circuits doubles every 18–24 months, page 1
multi-domain system	System containing circuits and devices which operations are based on different energy domains (*e.g.*, photonic, fluidic, electronic, mechanical,...), page 3
on-line test	Application of test during normal operation of a circuit, page 37
open defect	Unwanted impedance on a signal line that is supposed to conduct perfectly, page 21

passive fault	Fault which causes a incorrect behavior of the circuit and is independent on a state of the circuit, page 37
punchthrough	Extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region, page 48
rule of ten	Estimate of the cost associated with the defect detection which is ten times higher in each consecutive stage of production (*i.e.*, component, PC board, system), page 15
short defect	Unwanted impedance between any signal lines including power supply line and ground, page 21
stuck-at fault	Fault modeled by assigning a fixed (0 or 1) value to a signal line in the circuit affected by this fault, page 16
transition fault	Specific class of delay faults which causes passing transition to reach the output within a clock period, page 16
untestable fault	Fault for which no test can be found by a given test method, page 23
yield loss	Percentage of good chips classified as defective by testing and discarded, page 9

Chapter 1

Introduction

1.1 Overview

Over the last four decades the semiconductor industry has continued the expansion and improvement of its products. The ability to consistently improve performance while decreasing power consumption has established CMOS[1] technology as the dominant one for the production of integrated circuits. Aggressive scaling trends have brought about significant improvements in the following three domains: level of integration, operation speed, and power consumption. In essence, all of these improvements have resulted from our ability to exponentially decrease the minimum feature size of the MOSFET[2] device.

The most frequently cited trend is the integration level which is usually expressed as *Moore's Law*. The famous observation was initially made in 1965 by Gordon E. Moore, just six years after the invention of the first planar integrated circuit. In his original paper [127], Moore noted an exponential growth over time in the number of transistors per integrated circuit and predicted that this trend would continue. The law originally stated that the number of transistors per square inch on integrated circuits would double every year. In subsequent years, the pace slowed down, and in 1975, Moore revised his estimate for the expected doubling time to approximately 18 to 24 months. This trend has been maintained until today, and it is expected to continue at least through the end of the next decade [182].

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[1] Complementary Metal Oxide Semiconductor

[2] Metal Oxide Semiconductor Field Effect Transistor

Testing of integrated circuits is a crucial part of the complete chip manufacturing process. The purpose of the test process is to identify defective parts as well as parts prone to early failures, and, as a result, increase the quality and reliability of the product. Each silicon chip has to be individually tested before shipping to ensure the required quality/reliability levels. Product quality could be measured in a number of defective parts per million, whereas reliability can be defined as the probability that a product will continue to perform its intended function without failure for a specified period of time under stated conditions.

All scaling trends have huge implications for testing of *integrated circuits* (IC). Technology trends which enabled fabrication of a MOSFET device with a significantly reduced feature size, provided a foundation for an exponential increase in density, complexity, and operating frequency of integrated circuits. These trends, however, presented more complex test environments which resulted in the degraded capabilities of conventional specification or fault-model-based test methods and significantly higher manufacturing test cost. With continuing advances in the IC technology manufacturing processes, testing becomes more difficult and, inevitably, constitutes an increased portion of the total cost. Presently, the cost associated with the very large scale of integration (VLSI) IC testing already exceeds 50% of the total manufacturing cost.

1.2 Motivation – Trends and Challenges

Progressively greater IC complexity raises numerous new testing problems and exacerbates existing ones. The limitations of traditional testing methodologies demonstrate a critical need for the improvement in existing techniques and the development of alternative approaches. New and improved ways of testing are needed to deal with the ever-growing complexity of ICs, to meet stringent quality requirements, and to ensure product functionality.

Application of the test methodology as well as its implementation is primarily driven by the trade-off between the product test cost and test effectiveness. General trends in the semiconductor industry lead to the significant increase in test complexity and consequently test cost. The global technology trends which present the most significant challenges for integrated circuit test could be identified as follows:

- Increased operation frequency and clock rate;
- Integration of *heterogenous* and *multi-domain systems* on chip;
- Reduced accessibility to internal nodes, devices, and components;
- Scaling to devices with nano-meter features resulting in increased device density.

At-speed test, either functional or analog, continues to be utilized as an essential tool for the detection of design and process errors. However, at-speed test faces a major limitation in applications where increasing clock frequencies are approaching the multi-GHz range. Testing leading-edge digital and analog circuits require expensive high performance digital and analog automatic test equipment. As a result, the equipment and test time continue to dominate a total product test cost. Automatic test equipment (ATE), in spite of its very high cost, usually does not offer the memory capacities and test application speed required for testing of modern integrated circuits.

Technology development and scaling trends allow the integration of hundreds of millions of transistors on chip which will very soon result in multi-billion transistor systems. The integrated single-chip complex systems which may incorporate heterogeneous components (*e.g.*, logic, SRAM, DRAM, analog, mixed-signal, RF,...) as well as multi-domain non-electrical parts (*e.g.*, mechanical, fluidic, optical,...) are becoming a reality. Very often, different test equipment has to be used to cope with these highly integrated chip components.

At these levels of complexity, external testing using ATE is becoming extremely difficult. Beside the lack of high-speed interface circuits capable of transferring test information in and out of the chip, a significant challenge is presented by the reduced controllability and observability of circuit's internal components and nodes. To demonstrate this, the trend of rapidly increasing number-of-devices-per-pin ratio

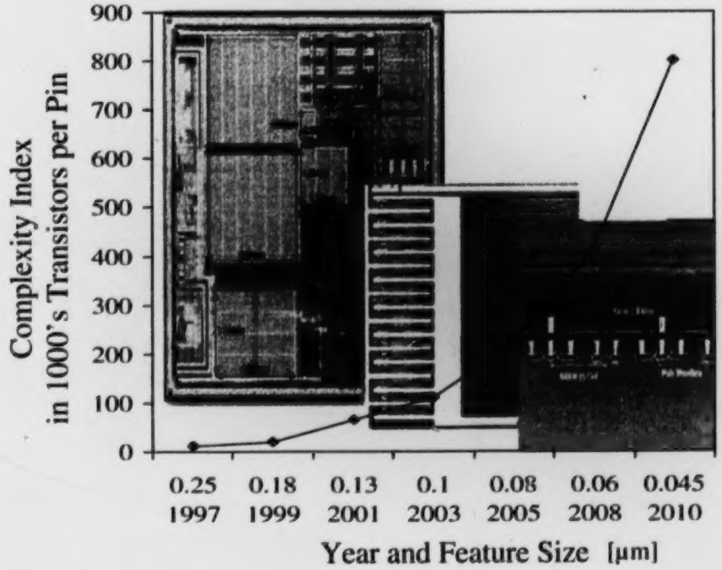

Figure 1.1: Complexity index trend

is shown in Figure 1.1. This figure is derived from the tables provided in [179]. The figure indicates an exponentially increasing number of transistors per pin, which translates to exponentially reduced access to individual devices. Comprehensive test strategies ultimately require a special test access to circuit's internal nodes.

Increased density and device size reduction, increased speed, and low power requirements are reducing noise margins and component reliability, increasing the impact and complicating the behavior of defects that could be represented by simple fault models in the past. The progress of semiconductor process technology is changing the population of physical defects that affect circuit functionality. Decreasing die size and increasing device density are causing dramatic increases in die thermal density which is driven even more by the exponential increase in leakage currents for sub-micron devices. These processes have a strong impact on failure analysis and reliability screens such as burn-in and current-based test.

Traditional test equipment based techniques need to be complemented with design-for-test based methodologies. Such methodologies require flexibility to effectively accommodate the mix of different circuit types on a single die or in a single package. Applications of such methods is needed to grow with the intention of moving test complexity on-chip which could reduce the capability requirements and cost of manufacturing test equipment.

1.3 Author's Contributions

The following summarizes the major contributions of this thesis:

- A novel current amplifying cell based on the application of the current conveyor;
- A new built-in current sensor amplifier topology suitable for current monitoring test applications;
- A design technique for improved variability-tolerant circuits based on the interpretation of the comprehensive characterization of the MOSFET drain current;
- A simplified resistive DC fault model of a MOSFET device for defect-based current test applications;
- A complementary defect-based test methodology for non-specification power supply current-based test for analog integrated circuits.

1.4 Thesis Organization

This thesis constitutes a comprehensive study of current-based test methodology, with emphasis of issues, requirements and potential solutions for embedded current-based test in deep sub-micron environments. A built-in current monitoring solution is identified as a potential opportunity to address the challenges by enabling easier access to the embedded core. In the process of developing a sensor device topology, we outline a set of requirements for successful application of embedded monitors.

Detailed analog behavior analysis of the proposed sensing device is presented, and the sensor is evaluated in a current monitoring testing scheme. Furthermore, the effect of process variations on device's current is investigated, and a methodology for non-specification current test of analog circuits is proposed. In the following paragraphs, we describe a thesis outline and topics covered in each of the chapters.

Chapter 2 provides the basic background information, terminology, and definitions needed for better understanding of the work proposed in this thesis. We introduce fundamentals of IC testing describing the test environments and concepts behind conventional IC testing including test objectives, stages, types, and methodologies.

Chapter 3 focuses on current-based testing as a methodology in testing of IC circuits. A historical perspective is presented along with elementary concepts behind this type of test. In this chapter, we place the emphasis on describing device leakage mechanisms in sub-micron technology processes. The motivation behind this effort is to understand the leakage properties of deep sub-micron transistors that are, beside design and performance related issues, also essential to guide effective solutions for current-based testing.

Chapter 4 elaborates on concepts and applications of power supply current monitoring[3]. We outline the requirements for the current monitor designs, and present different techniques for current sensing. We also explore existing methodologies and summarize different design concepts and principles of current sensing in test applications. A comprehensive survey of the relevant, state-of-the-art current monitor devices reported in the literature is provided in this chapter.

Chapter 5 presents a novel topology of the embedded current amplifying device. We describe a design and implementation of the novel built-in amplifier topology developed as a front-end device of a built-in monitoring system (*i.e.*, sensing and detection device).

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[3] *Power supply current monitoring* term used throughout this thesis refers to a particular aspect of current-based test specifically related to the accessing, sensing, amplifying, and processing of current power supply signals.

Chapter 6 investigates the feasibility, scope, and limitations of the current test technique for digital circuits based on the proposed built-in current sensing device which was presented in Chapter 5. The novel sensor topology is successfully employed in a current monitoring testing scheme. For verification purposes, the performance of the sensor design is investigated on several types of digital circuits.

Chapter 7 describes the effects of process variations on the drain current of a MOSFET device. In many analog CMOS circuits, a sum of drain currents constitute a significant portion of the total power supply current, which is a key parameter for current-based test. A comprehensive characterization of the drain current showing the scope of the variability due to the process variation has been provided. The results indicate that circuit design techniques could minimize to some degree rising process uncertainties and complement more advanced process techniques that reduce variability.

Chapter 8 explores a novel non-specification based test approach for analog circuits in a deep sub-micron CMOS process. The test method is based on power supply current measurements and is intended to be a part of the comprehensive test suite for early fault detection. The method targets non-catastrophic resistive open and short defects within the MOSFET devices.

Chapter 9 presents summaries and conclusions of the thesis. This chapter summarizes the topics covered in the thesis and briefly outlines the major contributions. Several topics in three main areas related to the work in this thesis are identified as opportunities for further research.

(no text)

Chapter 2

Fundamentals of IC Testing

2.1 Introduction

Semiconductor technology has enabled great progress in the design of complex integrated circuit systems. Many challenges in the manufacturing process had to be solved to achieve this. One of the steps in this process, namely testing, is posing the most significant challenge to contemporary and future integrated circuit manufacturing. This is a continuing trend, and due to decreasing silicon cost and increasing complexity of integrated circuits, testing constitutes a very sizable portion of the IC manufacturing cost [183].

The technology seeks to minimize the cost of IC testing, reduce a *defect level*[1] and *yield loss*[2] of fabricated semiconductor chips. Yield has become more important due to the sharp increase in competition, which has been enabled by more sophisticated computer-aided design (CAD) tools and advanced technologies. The semiconductor industry faces a pressure to cut costs as a result of falling prices and reduced profit margins. Since wafer prices and package costs are fixed, yield improvement is the best way to achieve this. For large and complex ICs, in order to maintain the same defect levels as for small chips, testing needs to be improved.

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[1] *Defect level* is a number of electrically significant defects per square meter. The targets for electrical defect density of DRAM, MPU, and ASIC necessary to achieve 83-89.5% chip yield could be found in [183], [182].

[2] Manufacturing *yield loss* occurs whenever any test or inspection process rejects as faulty a device that functions correctly. Causes of yield loss may include tester inaccuracies, mishandling, misprobing, *etc.*.

In the following subsections we introduce the fundamentals of IC testing as background information necessary for better understanding of the work proposed in this thesis. We describe the test terminology, environment, and concepts behind conventional IC testing including test objectives, stages, types, and methodologies, as well as IC test trends and challenges.

2.2 Stages of IC Testing

Depending on the purpose and the stage at which the test is performed, IC testing can be classified into four categories described below.

2.2.1 Characterization or Verification Test

Characterization or verification test is the most comprehensive test performed on new designs to verify that the design is correct and within specification, as well as to determine the limits of design operating conditions. The results of this test are usually used as a feedback to correct design errors. This test has to verify the product both from a physical as well as functional point of view, proving that it will be functional for the targeted product life and under the specified environmental conditions. This test might include AC and DC measurements, probing of internal nodes of the circuit, evaluation of the design behavior under different environment condition (*i.e.*, temperature, humidity, pressure,...) [18], [115].

2.2.2 Production Test

Production test is typically a short test performed on every fabricated chip that results in a pass/fail decision. It is less comprehensive than verification test but must enforce the required quality level of the designs manufactured in a particular fabrication run. The goal of any production test is to verify the device specification in the shortest possible test time, and therefore, to reduce the cost which is the main driver for production test [191], [148].

2.2.3 Burn-In

Burn-in is a portion of the test flow dedicated to the acceleration of dormant defects that do not appear as defects but could emerge as long-term reliability failures. Burn-in ensures the reliability of the fabricated chips. It is a screening process which mainly targets a potentially defective or 'weak' parts which have shorter live spans than the normal ones. Such parts cause early failures, often referred to as infant mortality failures. The burn-in process accelerates the aging of the part by exposing it to extreme operating conditions (temperature, voltage supply) and higher then usual level of stress for the extended period of time. Such conditions speed up the deterioration of materials or electronic components and exponentially accelerate the die failure rate [175]. There are many burn-in strategies. They can be undertaken at the wafer, die, package, or system level, and can involve single or multiple stresses [70], [88], [211].

2.2.4 Incoming Inspection

Incoming inspection of a chip is performed by the system manufacturers before integrating the chip into the system. It is established to precisely measure the quality of the received products and to ensure that only good material enters the production line. Incoming test strategies attempt to screen out defective parts at the earliest possible stage. The most important aspect of this test is to avoid placing defective chips into a system where the cost of diagnosis may far exceed the cost of incoming inspection [11], [187].

2.3 Types of IC Testing

Semiconductor fabrication involves several types of IC test depending on the manufacturing level at which the test is performed (processing, wafer, or package). Although some testing is done during device fabrication to examine the integrity of the process itself, most of the testing is performed after the wafers have been fabricated. The actual test selection depends on the specific application, manufacturer's test strategy, available test equipment, and test economics. In general, each chip is subjected to parametric and functional test.

2.3.1 Parametric Test

Parametric test measures physical and electrical parameters of the wafer and behavior of individual sample components. Parametric test is performed on special test structures which are designed to allow fast data collection and to diagnose production processes. A typical test structure could include MOSFETs, diodes, capacitors, resistors, bipolar junction transistors, insulation (oxide layers) and conductor (metallization) structures. The objective of this test is to identify small deviations and limits of operation which allow circuit commercial classification. Parametric test demands a longer time and a high-precision, complex measurement system. It includes DC test (*e.g.*, shorts, opens, maximum current, leakage, output drive current, threshold levels,...), and AC test (*e.g.*, propagation delay, setup time, hold time, functional speed test, access time, refresh time, rise and fall time,...) [196], [21].

2.3.2 Functional Test

Functional test determines whether or not individual IC components produce the expected responses. It consists of the input vectors and corresponding responses which are compared with the responses of the fault-free circuit. The test is intended to verify the functional capability of the device under a limited set of conditions. The cost of functional test is strongly dependent on the circuit complexity [18], [202].

2.4 IC Manufacturing Test Steps

An integrated circuit (IC) is an electronic circuit in which a number of devices are fabricated and interconnected on a single chip of the semiconductor material. According to the present manufacturing practice, integrated circuits are produced in the form of processed silicon wafers. While still in the wafer form, the ICs are re-

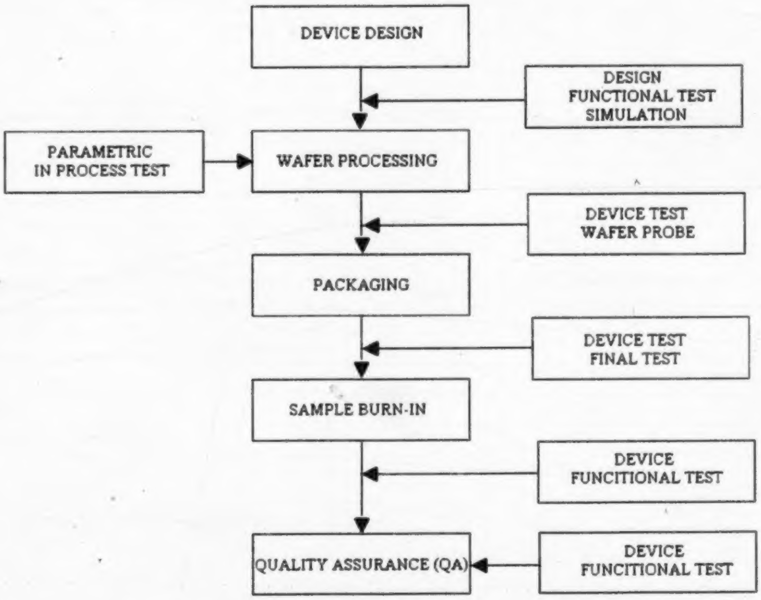
DEVICE DESIGN
DESIGN FUNCTIONAL TEST SIMULATION
PARAMETRIC IN PROCESS TEST
WAFER PROCESSING
DEVICE TEST WAFER PROBE
PACKAGING
DEVICE TEST FINAL TEST
SAMPLE BURN-IN
DEVICE FUNCITIONAL TEST
QUALITY ASSURANCE (QA)
DEVICE FUNCITIONAL TEST

Figure 2.1: IC manufacturing test steps [47]

ferred to as *dice*, and an individual IC is called a *die*. The process of cutting the dice from wafers and embedding them into mountable containers is called packaging.

Figure 2.1 describes major steps in IC manufacturing process flow with indication to IC manufacturing phases where those steps are usually performed. A bad device is considered any IC that fails to meet one or more specifications at any point of the process. Before fabrication, the design is developed using computer-aided-development (CAD) tools and designer verifies desired functionality through simulation.

During processing of the wafer, parametric testing is performed to determine the quality of the process and control process errors. Parametric tests measure physical and electrical parameters of the wafer such as the electrical conductivity and behavior of individual sample components (transistors, capacitors, resistors). Parametric tests are performed throughout the fabrication process.

Functional testing typically occurs once the wafers are completely fabricated and the dice are completely formed and functional. Functional tests measure the operational quality of the individual dice. A large and expensive robotic machine presses electrical probes onto the die contacts, input signals are fed to the circuit, and output signals are measured. Functional testing simulates normal and abnormal operating conditions (*e.g.*, high, normal, and low voltage tests). The conventional approach to die-level functional test (DLFT) is exhaustive wafer test, *i.e.*, all dice on all wafers undergo DLFT.

The main purpose of DLFT is to reduce costs by avoiding packaging defective dice. A secondary purpose of DLFT is to provide rapid feedback to the manufacturing process by detecting and diagnosing faulty manufacturing processes. A record of what went wrong with the non-working die is closely examined by the failure analysis engineers to determine where the problem occurred so that it may be corrected. If a die fails the functional test, an ink dot is placed on it, so that it will not be packaged later. In the case of inkless binning, a wafer bin map database is updated. Then, the wafers are typically shipped to a separate location for packaging.

To convert the wafers into packaged ICs, the wafers are cut into individual dice by a high-precision diamond saw. The resulting chips are mounted into packages, electrical contacts are bonded in place, and then a protective covering is added. Once the ICs are packaged, they are tested again to ensure that the packaging process was successful. A final test is performed to ensure proper handling, bond wiring, and packaging. Performance of the device is checked over the specific temperature range. Package tests usually repeat many of the functional tests that were performed during DLFT.

In the next step, the sample burn-in test is performed only on a selected set of IC's. This can be done, for example, using a higher temperature for an extended period of time. Before delivering the product to the customer, Quality Assurance (QA) test has to be performed. The need for standardization of QA test was driven by globalization in the microelectronics industry. The result of standardization was two popular ISO9000 and ISO9001 standards[3].

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[3] http://www.iso.org/

The main purpose of apparently redundant tests is to increase the probability of detection of defective devices in the early stages of manufacturing process. Experience has shown that the *rule of ten* [18] is used to describe the cost when a defective chip escapes early detection. Catching a defective device in each following step multiplies the original cost of manufacturing by an additional factor of ten. Finally, if a faulty device reaches the market, it leads to a damaged reputation and, ultimately, loss of market share.

2.5 Defects, Faults, and Fault Modeling

A *defect* is the physical imperfection in the implementation of the IC circuit. It could be a result of the manufacturing process but could also occur during the use of the device. At the chip level, defects could fall into many categories: interconnect defects, packaging defects, process problems, and so on. IC fabrication process is extremely complex and prone to imperfections such as local contamination, lattice shifting, incorrect masks, process errors, insufficient doping, silicon die stress, *etc.*. As a result, a large number of different physical defects can potentially occur in CMOS circuits. Some common silicon CMOS defects are: gate-oxide shorts, metal trace resistive opens, metal trace resistive bridges, anomalies in vertical interconnections between metal layers (open or plugged vias), shorted or broken metal lines, incorrect threshold voltages, *etc.*. Defects have very complex physical characteristics and may be significantly different from the simplistic defect models assumed by typical fault modeling techniques.

A *fault* is a representation of a defect at the higher level of abstraction. Through the abstraction process, a fault model maps a large number of defects into smaller number of modeled faults. A fault can be viewed as the failure-mode manifestation of the defect. For example, a gate-oxide physical imperfection could effectively short the gate and drain of a transistor. Such a defect can be represented as a transistor-level gate-to-drain short fault. Another example of a defect mapping to a fault is the small metal open on a connection trace. In this case, the logic value can still propagate, but only by a tunneling current across the open. As a consequence, the propagation of the logic value is slowed as if it were passed through a series resistance. The fault model at the circuit level is to represent the defect as a unit of signal delay along the length of the signal trace. This fault model is generally known as a *delay fault* [136].

Fault modeling is the translation of physical defects to a mathematical expression that can be operated upon algorithmically and understood by a software simulator for the purposes of providing a metric for quality measurement. The purpose of fault modeling is to augment and generalize the analysis of the behavior of the system in the presence of a defect. It is the way to bridge the gap between the physical reality and the abstraction level through which we can apply analytical methods and develop overall test strategy for cost effective IC test. The selection of the adequate fault model is crucial to achieving a high quality of testing.

Faults could be modeled at different abstraction levels. For example, a behavioral fault model has fewer implementation details, and fault models at this level may have no obvious correlation to manufacturing defects. On the other hand, faults modeled at the gate or transistor level, such as shorts or opens, are sometimes referred to as *defect-oriented faults* since they represent defects modeled by the faults at the physical level [18]. Some of the most common fault models supported in modern VLSI and core-based digital design are the single *stuck-at fault* DC model, *transition fault* model, and path *delay fault* AC model.

2.6 Die Failure Mechanisms

There are numerous mechanisms of semiconductor *failures* [52], [56]. Generally, they could be classified into three groups: intrinsic (process induced) failures, extrinsic failures, and operating-environment-related failures.

Failures inherent to the semiconductor die itself are defined as intrinsic. Intrinsic failure mechanisms tend to be the result of the wafer fabrication which is the front-end of the manufacturing process. Intrinsic failures including crystal defects, dislocations, spot defects, mask misalignments, processing defects, ionic contamination, and surface charge spreading are only few of many examples of intrinsic failure mechanisms. Foundries invest a great effort to control the above fabrication related failure mechanisms by designing a fabrication process which minimizes unnecessary stresses applied to the wafer and maintains environment cleanliness to eliminate contamination [91], [109], [41], [188].

Extrinsic failures result from device packaging, metallization, bonding, die attachment failures, particulate contamination, and radiation of semiconductor manufacturing. Extrinsic conditions affecting the reliability of components vary according to the packaging and interconnection processes of semiconductor manufacturing [91]. In the following paragraphs we outline most common operating-environment-related failure mechanisms [54], [55].

2.6.1 Electromigration

Electromigration (EM) is a mass transport due to momentum exchange between conducting electrons and diffusing metal atoms. It causes progressive damage to the metal conductors in an integrated circuit. It is characteristic of metals at very high current density and high temperatures. Eventually, EM leads to catastrophic and irreversible breakdown. As the technology scales down, the wires become thinner and more prone to EM effect. Most technologies today use copper instead of aluminium in order to reduce interconnect resistivity and minimize the effects of electromigration [135].

2.6.2 Hot-Carrier Injection

Hot-carrier injection (HCI) stems from large electric fields below the gate oxide, which allow electrons to gain energy and embed themselves in the dielectric. With designs moving into deep sub-micron levels, shorter channel lengths cause the electric field in the channel to become larger. This causes more electrons to become energetic or "hot". Some of these hot electrons will damage a channel-oxide interface and lead to circuit performance degradation [48]. The HCI effect contributes to the total leakage current of short channel MOSFET devices. We discuss it in more details in Chapter 3, Subsection 3.4.8, on page 56.

2.6.3 Electrical Over-Stress

Electrical over-stress (EOS) results in the circuit destruction because of excessive voltage, current, or power. A typical EOS damage involves discolored, burnt, or melted metal lines. Improper excitation settings or voltage spikes in the excitation source are common causes of EOS damage. EOS damage is not always obvious though. Some EOS events leave no apparent physical manifestation on the die surface at all. Such EOS events can still render the affected component non-functional even if no physical anomalies are observable. Weak EOS events may shift the parametric performance of the affected component which can affect the overall performance of the device.

2.6.4 Junction Burn-Out

Junction burn-out is a destruction of a p-n junction as a result of excessive power dissipation from an electrical over-stress (EOS) or electrostatic discharge (ESD) event [48], [210]. It is usually in the form of a silicon meltdown at the junction itself, causing the junction to become open or shorted.

2.6.5 Dielectric Breakdown

Dielectric breakdown refers to the destruction of a dielectric layer, usually as a result of excessive potential difference or voltage across it. It is usually manifested as a short or leakage at the point of breakdown. The permanent breakdown of an oxide dielectric is also usually referred to as *oxide rupture* or *oxide breakdown*. The most common cause of dielectric breakdown in devices is electrical over-stress (EOS) or electrostatic discharge (ESD). Both of these events can expose the dielectric layer to high voltages [117], [193].

2.6.6 Metal Burn-Out

Metal burn-out implies the total destruction of a metal line from excessive current or high power dissipation. This is the most obvious manifestation of the gross electrical overstress (EOS) damage, although not all EOS-damaged devices exhibit a metal burn-out. Metal burn-out is often accompanied by carbonized plastic and discoloration of the metal around it. Metal lines may become open after metal burn-out.

2.6.7 Slow Charge Trapping

Slow charge trapping refers to the long-term retention of electrons in the gate oxide of a MOSFET device due to the presence of imperfections in the gate oxide interface. These imperfections or traps include structural damage, defects, and impurities in the oxide. Trapped charges in the oxide can shift the threshold voltage of the device. Improved oxide growth to minimize trap density will minimize the occurrence of slow trapping. Slow trapping is prevalent in EEPROM[4] memory devices that require carrier movement through the oxide for proper operation [137].

2.7 Opens and Shorts

In the previous paragraphs, we defined the terms *defect*, *fault*, and briefly introduced most dominant failure mechanisms. Numerous failure mechanisms produce defects which manifest themselves as open and short faults. For example, gate-oxide breakdown close to the drain-gate/source-gate overlap could effectively short the gate and drain/source of the MOSFET device. Similarly, a spot defect due to the impurity of the process could bridge two neighboring interconnection lines. Alternatively, the effects of electromigration could lead to the breakdown of a metal conductor making it either open circuit or series resistive line. Due to the high occurrence probability of open and short defects in IC circuits, consideration of such defects as well as their realistic and effective modeling is a crucial part of a successful defect detection process. Sample micrographs of the actual IC defects are shown in Figure 2.2.

Opens and shorts are the faults which could be modeled at the gate or transistor level. Since they are faults produced by failure mechanisms and map closely the

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[4] Electrically-Erasable Programmable Read-Only Memory

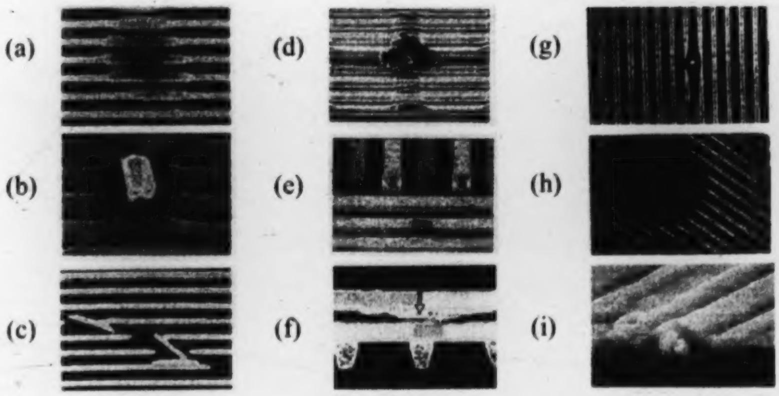

Figure 2.2: Micrographs of short and open defects [146]: a) Bridging of seven metal lines caused by unexposed photoresist; b) Shorting of four metal lines by a particle on the metal mask; c) Shorts and opens of metal lines caused by a scratch in the photoresist; d) Short among multiple metal lines by a metallization defect of 1 μm in size; e) Short between two Al lines due to metallization defect; f) Inter-layer short between two Al interconnects in 0.5 μm technology; g) A foreign particle causing a line open and a line thinning; h) A contaminating particle causing 7-line opens; i) A defect which caused an open in metal 2 and a short in metal 1.

actual physical defects, opens and shorts are also classified as *defect-oriented faults* [18]. In the literature, they are usually referred to as defects [173] or faults [100] depending on the level of abstraction at which they are modeled. Nevertheless, exceptions to this rule can also be found [222].

2.7.1 Open Defects

An *open defect* [126], [20] represents unwanted impedance between two nodes on a signal line that is supposed to conduct perfectly. For the open defect, the impedance value is predominantly resistive. The resistance of such a defect may have any value. A *catastrophic open* assumes infinite resistance between its nodes. The fact that open defects generally result in negligible capacitive coupling between the broken nodes has been substantiated by Henderson *et al.* [57]. Open defects within MOSFET device can cause the gates of transistors to be disconnected from the rest of the circuit. The behavior of the devices with such defects, known as *floating gate* transistors, has been studied in [67], [152].

2.7.2 Short Defects

A *short defect* (also called *bridge*) represents unwanted impedance between any signal lines including a power supply line and ground. For a short defect, the impedance value may have resistive and capacitive components. The resistance may have any value, while the capacitance is bounded by some given realistic limits. A *catastrophic short* assumes zero resistance between its nodes. Due to the nature of failure mechanisms which cause short defects, it is highly unexpected for the parasitic capacitance to have a high value [100]. In the experiment conducted by Rodríguez–Montañés *et al.* [159], the authors found that the majority of bridges have resistances below 500 Ω, and only small percentage of them have a resistance between 500 Ω and 2 kΩ.

2.7.3 Gate-Oxide Short Defects

A gate-oxide short (GOS) is a defect causing a low impedance between the gate and one of the other regions of a MOS transistor (drain, source, or substrate). The relative impact of GOS in the quality of ICs with very low expected defect levels and high reliability is a key issue. Among the wide set of possible failure mechanisms in ICs, the one which produces a GOS defect is the breakdown of the gate oxide which has been the dominant mechanism failure for CMOS ICs [173], [153], [50].

The analysis of this defect behavior is a complex problem. One of the main challenges comes from the uncertainty of the defects' parameters, preventing accurate prediction of the defect behavior. The mechanisms of the defect appearance are obviously not controlled, resulting in electrical situations with unknown parameters. A challenging but realistic model of defect behavior should incorporate the random parameters. Using a simple example of a catastrophic short or open defect in fault modeling is not sufficient for comprehensive defect-based test.

2.8 Functional vs. Structural Testing Strategy

Functional test has the goal to determine if a unit functions properly. An exhaustive functional test assumes a complete set of all input signal patterns which fully test a circuit function. This is the best test for any device since any defective IC would be identified. However, even for circuits with a relatively small number of inputs and/or type of input signals, this kind of testing becomes impractical and very often impossible due to a number of practical limitations including: limited tester memory, limited test application time, *etc.*. Functional testing alone cannot offer the quality and defect coverage required for today's integrated circuits.

Structural test methods offer an alternative to exhaustive functional test. Rather than test for the correct operation of the complex function, structural test targets defects through a selected fault model. Depending on the type of fault model and its abstraction level, the structural test could uncover defects within the gates, devices, and interconnects within them. ***Defect-based test*** (DBT) is a structural test method which targets physical defects via more realistic, less-abstract fault models. The primary motivation in augmenting structural testing with DBT is to make up for some of the potential quality losses in migration to structural test methods as well as to meet the challenges of sub-micron defect behavior. Although the impact of DBT on defects per million products shipped is not well characterized, many studies of DBT show that it improves product quality.

In comparison to functional test, structural test uses a smaller set of test patterns generated to detect targeted faults. In this way it is possible to achieve high test quality with increased efficiency of the test resources, resulting in a significantly reduced cost of test [76]. A minimal set of modeled faults is found after discarding *equivalent faults* in a process known as *fault collapsing*. Faults are partitioned into classes and only one fault per class is considered in the fault simulation and test generation analysis [102], [113].

2.9 Fault Metrics

Fault coverage is a common metric used in the testing of IC circuits. It is an accepted measure of the quality of an IC test, and is defined as the percentage of the ratio of the number of detected faults over the total number of all possible faults.

$$Fault\ Coverage[\%] = \frac{Number\ of\ Detected\ Faults}{Total\ Number\ of\ Faults} \cdot 100 \qquad (2.1)$$

Sometimes, the total number of faults in the design is not used as the denominator of the measurement process, but is reduced by the number of *untestable faults* which cannot be detected by any input test pattern. Such an approach might not produce a reliable and meaningful fault coverage measure [1].

In some cases, it is more meaningful to quantitatively evaluate the effectiveness of the test using *fault efficiency*. Fault efficiency is introduced as an alternative metric to the fault coverage to avoid a declining value of coverage due to the untestable faults. Fault efficiency is defined as the percentage of detected faults for all testable faults.

$$Fault\ Efficiency[\%] = \frac{Number\ of\ Detected\ Faults}{Number\ of\ Testable\ Faults} \cdot 100 \qquad (2.2)$$

2.10 Generation of Test Patterns

The objective of (automatic) test pattern generation (ATPG) is to find a set of input signals which, when applied to the circuit under test, enable a tester to distinguish between the correct and faulty circuits. The effectiveness of the test sequence is measured by the achieved fault coverage and the number of generated vectors/signals, which is directly proportional to the test application time.

Selected test signals enable a fault detection process which consists of two phases: fault activation and fault propagation. A test sequence can not be successfully performed unless the signal paths are available to enable both fault activation (controllability) and fault propagation (observability). Fault activation attempts to establish a signal value at the fault site different of that produced by the fault. Fault propagation transports the fault effect from the fault site to the outputs [18].

2.11 Design for Testability

Design-for-testability (DFT) is the most important aspect of IC design and test. It is a part of the design process with the objective of improving the testability of an IC. DFT could be defined as adding logic, circuitry, or features to a design in order to enable or enhance the ability to achieve high quality test metrics. It is a way to ease the generation of test signals, to minimize the time involved with the test application, and to reduce the overall cost associated with the test. DFT assumes special implementation techniques which enable controllability and observability of IC's internal nodes, and, as a result, enable development of high fault coverage test programs which can efficiently and quickly test an IC.

There are numerous DFT implementation strategies. They can be either ad-hoc or structural [47]. Ad-hoc DFT methods rely on good design practices but are not suitable for large or deeply integrated circuits. Structural DFT approaches are supported by the extra circuitry which allows access and test according to some predefined procedure. Some of the structural DFT methods are developed to target specific types of circuits, *e.g.*, digital [203], analog/mixed [154], and memory [142]. In the following sections, we identify commonly used structural DFT approaches.

2.11.1 Full Scan

Full scan is a structured design approach where all of the internal latches are configured into one or more shift registers. In this way, the values of connected memory elements can be controlled or observed during the test mode by shifting the desired values into the register or shifting the content out of the register. This ensures controllability and observability of all the latches. Scan designs dramatically reduce the complexity of testing at the expense of a larger chip area because of converting regular flip-flips into larger scan flip-flops. As a result, the latches become tools for the purpose of test applications and observations. A full-scan design is often considered the best DFT approach [18], [134]. However, the test application time increases as the length of the scan chain increases.

2.11.2 Partial Scan

Partial scan is an alternative to full scan. Instead of creating shift registers using all internal latches, only some selected flip-flops/latches are scanned. Usually, memory elements with poor controllability are selected for scan. The objectives of this approach are to minimize the area overhead, improve performance, shorten the scan sequence length, and achieve required fault coverage. Partial scan provides a tradeoff between the ease of testing and the costs associated with scan design. However, the key problem in partial scan design is the selection of scan registers. Although a non-scan flip-flop or latch might be slightly smaller and have a slightly faster setup time than its full scan equivalent, any potential advantages of partial scan design must be carefully evaluated [134].

2.11.3 Boundary Scan

Boundary scan is a DFT approach that can be utilized at the board level, IC component level, or system level. It consists of placing scannable latches adjacent to all chip's primary inputs and outputs as shown in Figure 2.3. These latches are called boundary scan cells which permit control of primary inputs and observability of primary outputs. The boundary scan architecture has developed into the industrial standard IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-2001 [65], [8], [218]. This standard defines the test logic that can be included in an integrated circuit to provide standardized approaches to:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate;
- testing the integrated circuit itself;
- observing or modifying circuit activity during the component's normal operation. The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

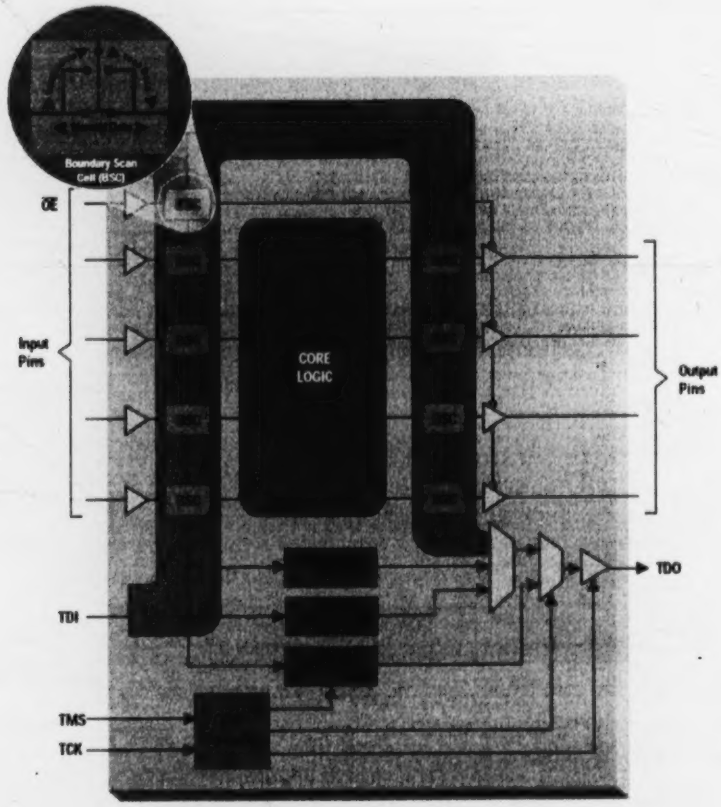

Figure 2.3: Boundary-scan architecture uses a boundary-scan cell (BSC) at every I/O pin which can interrupt normal data, sample data and inject test data according to the IEEE 1149.1 instruction set.

The circuitry defined by this standard (Figure 2.3) allows test instructions and associated test data to be fed into a component and, subsequently, enables the results of execution of such instructions to be read out. All information (instructions, test data, and test results) is communicated in a serial format. The sequence of operations is controlled by a bus master, which could be either an automatic test equipment (ATE) or a subsystem that interfaces to a higher-level test bus as a part of a complete system architecture. Control is achieved through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) inputs of the various components connected to the bus master.

Starting from an initial state in which the test circuitry defined by this standard is inactive, a typical sequence of operations would be as follows. The first step would be to load serially into the component the instruction binary code for the particular operation to be performed. Once the instruction has been loaded, the selected test circuitry is configured to respond. In some cases, however, it is necessary to load data into the selected test circuitry before a meaningful response can be made. Such data is loaded into the component serially in a manner similar to the process used previously to load the instruction. After execution of the test instruction, the results of the test can be examined by shifting data out of the component to the bus master. In cases where the same test operation is to be repeated with different data, new test data can be shifted into the component while the test results are shifted out. There is no need for the instruction to be reloaded. Operation of the test circuitry may proceed by loading and executing several further instructions in a similar manner and would conclude by returning the test circuitry and, where required, on-chip system circuitry to its initial state.

This standard has been widely adopted by the semiconductor industry, and the boundary scan architecture has become a part of almost every large-scale IC including microprocesors (MP), digital signal processors (DSP), application-specific integrated circuits (ASIC), and systems-on-chip (SoCs).

2.11.4 Mixed-Signal Test Bus

The mixed-signal test bus (IEEE 1149.4 standard) is an extension of the IEEE 1149.1 standard and consists of additional structures which support analog test operations to be performed in a consistent and coordinated manner [64], [74]. The overall structure of a component which conforms to the basic IEEE 1149.4 standard is illustrated in Figure 2.4. The aim of the test structures described in this standard is to provide test access to individual component pins, and to reduce or eliminate the need for the ATE to make direct physical contact via mechanical probes. However, the standard doesn't eliminate the need for an analog tester. The standard defines

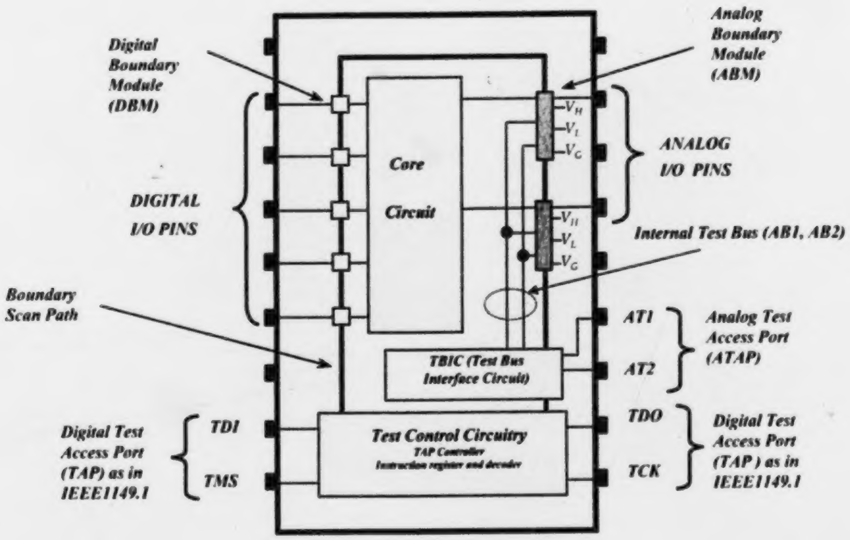
Digital Boundary Module (DBM)
Analog Boundary Module (ABM)
Core Circuit
V_H
V_I
V_G
V_H
V_L
V_G
ANALOG I/O PINS
DIGITAL I/O PINS
Internal Test Bus (AB1, AB2)
Boundary Scan Path
AT1
AT2
Analog Test Access Port (ATAP)
TBIC (Test Bus Interface Circuit)
TDI
TMS
TDO
TCK
Test Control Circuitry
TAP Controller
Instruction register and decoder
Digital Test Access Port (TAP) as in IEEE1149.1
Digital Test Access Port (TAP) as in IEEE1149.1

Figure 2.4: Mixed-signal test bus standard architecture with a minimally configured component

test features to be included in a mixed-signal (analog and digital) component, together with associated test protocols, to provide standardized approaches to

- testing for opens and shorts among the interconnections;
- making passive elements characterization measurements (parametric test);
- testing the internal circuitry of the mixed-signal component itself.

Mixed-signal test bus consist of analog boundary modules (ABMs) for every analog function pin, allowing access for analog test signals through the analog test access port (ATAP) which consists of two pins (AT1 and AT2), a test bus interface circuit (TBIC), and an internal analog test bus with two lines (AB1 and AB2). The boundary modules associated with the digital pins are identical to the boundary cells, or groups of boundary cells, as specified in IEEE 1149.1. Boundary modules on analog pins form the main subject of this standard, in which they are mandatory.

Each ABM has associated with it a set of voltages (V_H, V_L, and V_G) needed to drive analog pins for interconnect tests.

Part of the manufacturing process for semiconductor wafers is the inclusion of the 'process monitors' on the wafer. These monitors consists of group of transistors with sufficient probing access to characterize the parameters. The probe pads consume most of the area required by process monitors. This standard can provide significant wafer area savings by eliminating the area associated with probe pads and provide better wafer test information after the part is packaged, while the component is assembled on the board, or after the component is removed from the board for failure analysis. Besides the benefits, the mixed signal test bus has several limitations such as inherent measurement error, limited linearity of the interface circuitry, and the limited bandwidth of the system [205].

2.11.5 Built-In Self-Test

Built-in self-test (BIST) is the capability of a circuit, chip, board, or system to test itself. A BIST scheme incorporates the additional circuitry to the design which is capable of generating test signals on-chip, applying them to the circuit, and processing the responses.

BIST is beneficial in many ways. It provides better test access, fault detection and diagnosis, higher yield, improved design and verification, shorter time-to-market, lower test program development costs, reduced test time, and design and test reuse. In addition, BIST can overcome pin limitations due to packaging, make efficient use of the available extra chip area, and provide more detailed information about the faults. BIST is an attractive test solution since it allows at-speed testing (*i.e.*, test at the intended operating speed of the circuit), thus solving timing accuracy and test time related problems encountered with traditional external testers. Moreover, BIST drastically reduces the amount of test data exchanged with the tester, which greatly minimizes or even eliminates the need for complex external testing equipment. Finally, BIST may relieve the tester memory capacity problem and the problem of poor accessibility to internal nodes inside the design. On the other hand, implementation of the BIST undoubtedly incurs an area overhead, performance penalty, and increased design effort and time. Therefore, BIST application costs vs. benefits should be carefully evaluated in each particular situation [204].

Specific implementation of the BIST designs depends on the type of test and the type of the circuit which is subjected to test. Numerous BIST implementation solutions have been proposed. Although the BIST concept originates from digital and memory circuits where it is presently widely used, techniques for applying BIST ideas to analog, radio-frequency (RF), and mixed-signal devices have recently been attracting considerable industrial interest in attempt to alleviate increasing test related difficulties. Related research has been presented in the area of RF BIST [104], [209], mixed-signal BIST [197], [145], analog BIST [59], [207], logic built-in self-test (LBIST) [58], [31], and memory built-in self-test (MBIST) [223], [18].

Design-for-test methodologies provide a platform for the efficient application of a variety of test techniques for integrated circuits. The new failure modes being observed in the present generation of IC circuits raise an important question: Can traditional test strategies, built around existing fault models, meet the test challenges in emerging deep submicron technologies, or do we have to increasingly rely on defect-based test methods that directly target physical defects? The answer to this question must be given in the context of current-based testing as defect-oriented testing which has the strong potential to better handle emerging defect types in nanometer devices compared to conventional test. In the next chapter, we introduce current-based testing.

Chapter 3

Current-Based Testing

3.1 Introduction

The ability to observe and measure the supply current flow within an integrated circuit has proven to be a useful means to detect defects and improve testability. The fundamental principle of the current-based test method for CMOS circuits assumes that defective circuits consume a measurable and significantly different amount of supply current compared to the current consumed by the defect-free circuits. In the presence of defects, the level and the wave shape of the supply current changes, providing us with a tool to detect a faulty device. Over the last two decades, current-based testing has progressed to become a worldwide accepted test method to detect IC defects in CMOS circuits. The value of current-based test such as quality improvement, test cost reduction, and burn-in elimination have been well recognized [53], [116].

3.2 Historical Perspective

Frank Wanlass at Fairchild Semiconductor[1] proposed and published the idea of the CMOS circuit topology [214]. He noticed that a complementary circuit including NMOS and PMOS transistors consumed very little current under steady state conditions. A CMOS topology shrank standby power by several orders of magnitude over equivalent bipolar or PMOS logic gates. On June 18, 1963 Wanlass applied for a patent which was issued four and a half years later for 'Low Stand-By Power Complementary Field Effect Circuitry'. Today, CMOS forms the basis of the vast majority of all high density ICs.

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[1] http://www.fairchildsemi.com/

Since the inception of the semiconductor industry, current-based test has been an important part of the IC testing process. It has been used to detect catastrophic short circuit defects (shorts) and has been generally referred to as static I_{DD} test. With the invention of the CMOS circuit topology, the current-based test expanded further. The inherent property of the CMOS logic is a low current in its static state. This property was a foundation on which researchers developed a new current-based test methodology. The present form of quiescent current-based test for CMOS circuits, known as I_{DDQ} test, was first publicly proposed by Mark W. Levi in 1981 [99]. The initial idea has evolved further, and by the mid 1980's, I_{DDQ} test was recognized as an effective means to detect physical defects such as bridges and gate oxide shorts in CMOS logic circuits.

In the early stages of I_{DDQ} test development, beside government and defense labs, few commercial semiconductor manufacturers included I_{DDQ} test as a part of their overall test suite. At that time, static I_{DD} test was mainly used in the semiconductor industry. Although this type of current test could be regarded as a single I_{DDQ} measurement, it is identified by a different name (static I_{DD} test, I-test, easy current test, *etc.*) and considered separately from I_{DDQ} testing which implies multiple current measurements. By the mid 1980s, semiconductor manufacturers started to recognize I_{DDQ} testing as an effective means to detect physical defects [146].

Even before the CMOS technology became the mainstream, semiconductor companies were aware of the limitations of the stuck-at fault model and the fact that many physical defects were not adequately described by this model. Conventional testing in the voltage domain was not sufficient to provide required quality standards, and testing methods which target layout-dependent, process-oriented defects were needed.

7

The defect-oriented simulation approaches, such as *inductive fault analysis*[2], clearly showed that many defects were not well represented by existing stuck-at fault models, and were not detected by the conventional testing [32], [69]. This became even more evident as the minimum feature size of the MOSFET device was scaled down below 1 μm. Particle (spot) defects became the dominant cause of failure [109].

As defect-oriented test, I_{DDQ} has gained a wider acceptance in the semiconductor industry. I_{DDQ} testing is seen as not only a supplement to the functional/logic testing but also an important part of reliability testing [144], [53]. I_{DDQ} test requires little work by the circuit designer, negligible or no area overhead or increase in die size, and only a small number of vectors in the I_{DDQ} test set. In the mid 1990s, a number of studies were conducted to correlate the effectiveness of I_{DDQ} testing with conventional reliability screenings (stress testing) and burn-in [53], [155], [12], [77]. Many companies started using I_{DDQ} testing as a supplement to reliability screening, which reduced standard burn-in time and resulted in a higher quality of their products [146], [108], [144]. I_{DDQ} test plays a key role in defect-based testing necessary to meet the challenges presented by the technology scaling.

3.3 Power Supply Current Test Concepts

During the last decade a lot of research work has been done to further develop and improve current-based test methodology and extend its application versatility. As a result, a variety of current-based test methodologies have been proposed and utilized in the semiconductor industry.

A typical pattern of the power supply current during the operation of a CMOS digital or mixed signal circuit is shown in Figure 3.1. In general, two components can be distinguished: quiescent, I_{DDQ}, current and transient, I_{DDT}, current. I_{DDQ}

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[2] *Inductive fault analysis* (IFA) is a systematic method for determining the realistic faults likely to occur in a VLSI circuit. This method takes into account the circuit's fabrication technology, fabrication defect statistics, and physical layout. The inductive approach of characterizing faults, by drawing conclusions based on analyzing the particulars of low level fault-inducing mechanisms, departs from the traditional scenario of simply assuming a convenient high-level fault model.

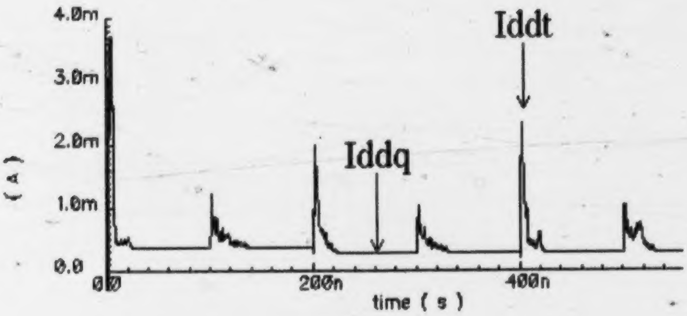

Figure 3.1: Power supply current components

current is leakage current, also called background or off current. I_{DDT} current is produced by the circuit during the transition period. Current-based test can effectively exploit either of the two components as a tool for defect detection and, as such, it is called I_{DDQ} or I_{DDT} test. The following paragraphs present fundamentals of each methodology as well as a brief overview of different test approaches.

3.3.1 I_{DDQ} Test

I_{DDQ} test is a defect-based test that measures the device supply current under steady state conditions. In a stable state, fully static CMOS circuits consume very little power which is due to the leakage current only. The basic principle of I_{DDQ} test is founded on the concept that defective circuits produce an abnormal or at least significantly different amount of supply current compared to the current produced by the defect-free circuits. Such defects may have a direct influence on the functionality of the circuit (functional failure) or may negatively affect the lifetime and reliability of the circuit (early-lifetime or *infant mortality* failure) [12], [212].

The basic premise of I_{DDQ} test could be clearly understood with the help of the simple CMOS NOR gate circuit shown in Figure 3.2. As indicated, this NOR gate contains a gate-oxide defect which effectively shorts the source and the gate of the PMOS transistor. Figure 3.3 displays how this defect affects the power supply current. Two waveforms compare I_{DDQ} currents of the defective and defect-free

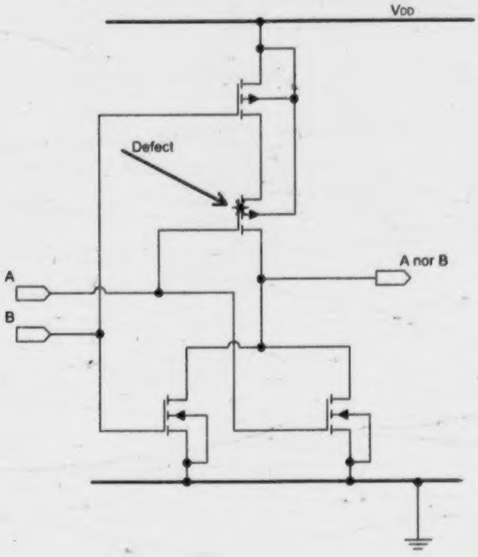

Figure 3.2: Defective NOR gate

NOR gate. When inputs $A \neq 0$ or $B \neq 0$, stable state quiescent currents drawn from the power supply are identical in both cases since a defect in PMOS device is not activated (*i.e.*, two nodes connecting the defect are not driven to the opposite voltage levels). The input combination $A = 0$ and $B = 0$ activates the defect by establishing a low resistive path between V_{DD} and ground which conducts current proportional to the resistance of the defect. With 1.2 V power supply, 50 kΩ defect resistance elevates total I_{DDQ} for 24 μA. This additional current clearly signals a defective circuit.

Defective chips usually have the level of the supply current measurably different from the defect-free devices. I_{DDQ} current of the manufactured chips is intrinsically statistical and could be approximated by the normal distribution. Therefore, the mean and standard deviation are two important parameters to be considered when a line is to be drawn between the I_{DDQ} currents of good devices and defective devices. The ideal distribution of the I_{DDQ} values for a collection of faulty and fault-free chips is shown in Figure 3.4. The first normal segment of the distribution depicts the

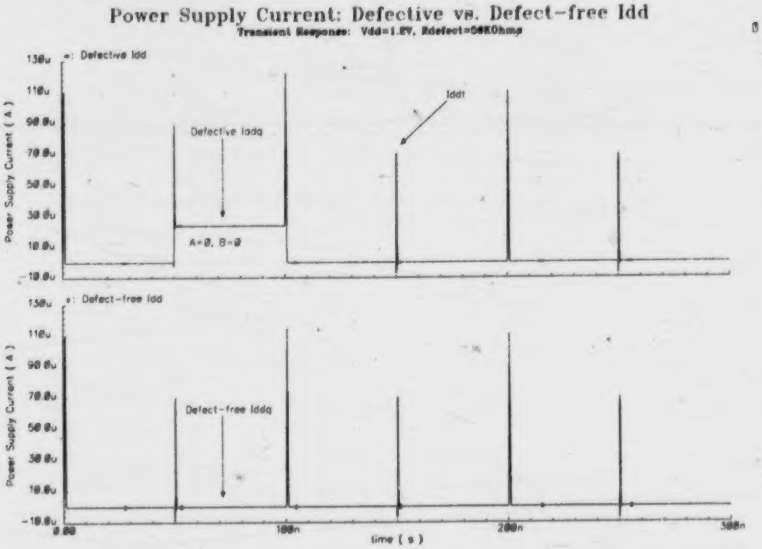

Figure 3.3: Faulty and fault-free I_{DDQ} current

I_{DDQ} values in the good product. At the high end of the I_{DDQ} values, another normal distribution appears as a result of some of the defective parts drawing excessive current from the power supply. If a current threshold can be established between the two segments of the distribution which separates the good and the defective product, a potentially efficient test may be obtained. Any CMOS IC that falls below the threshold is classified as good product while those above the threshold are classified as defective product.

The positioning of this threshold is very important in an I_{DDQ} test methodology. If the threshold is too close to the mean for the good product, a significant number of good parts may be wrongly classified as defective; this translates to a loss of yield making the test uneconomical. Moving the threshold to higher I_{DDQ} values may result in ineffective I_{DDQ} tests. Thus, for I_{DDQ} testing to be successful, it is very important that the means of the two normal segments of the distribution be separated by a significant amount [216].

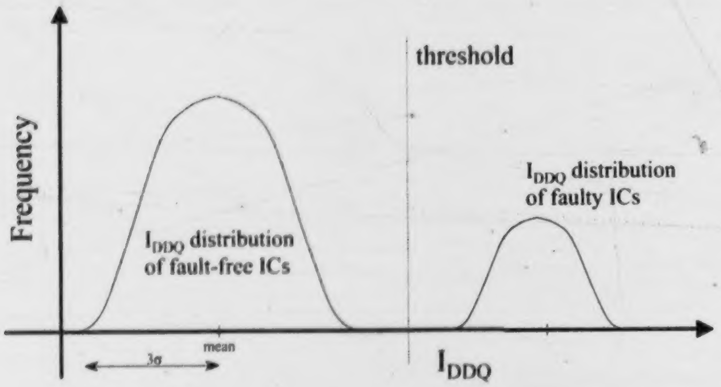

Figure 3.4: Faulty and fault-free distribution of I_{DDQ} current values

I_{DDQ} test is most effective in detecting catastrophic or resistive shorts (bridges) between two switching nodes or a signal and power supply line (both categories referred to as an active or pattern-dependent defect/fault[3]), or between V_{DD} and ground (called a passive or pattern-independent defect/fault). An *active fault* increases the leakage for some (but not all) input patterns while a *passive fault* increases leakage for all input patterns. An active defect degrades functionality of a chip (due to reduced noise margin, *etc.*). For this reason, several I_{DDQ} test methods are targeted towards discarding chips with active defects. Passive defects may not affect the functionality of the circuit. However, as previously mentioned, they present a reliability concern.

The I_{DDQ} test technique can be applied at the wafer level, at packaged device level, during incoming inspection, during life tests or even as *on-line test*.

3.3.2 I_{DDT} Test

The current consumption of CMOS digital circuits exhibits sharp transient current peaks that appear during switching activity of the circuit. Certain defects might cause transient current of a defective circuit to be different from a defect-free one [90], [167]. Even though only I_{DDQ} techniques have been used in practice, it has

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[3] In the literature, *defect-oriented faults* are interchangeably referred to as *faults* or *defects*.

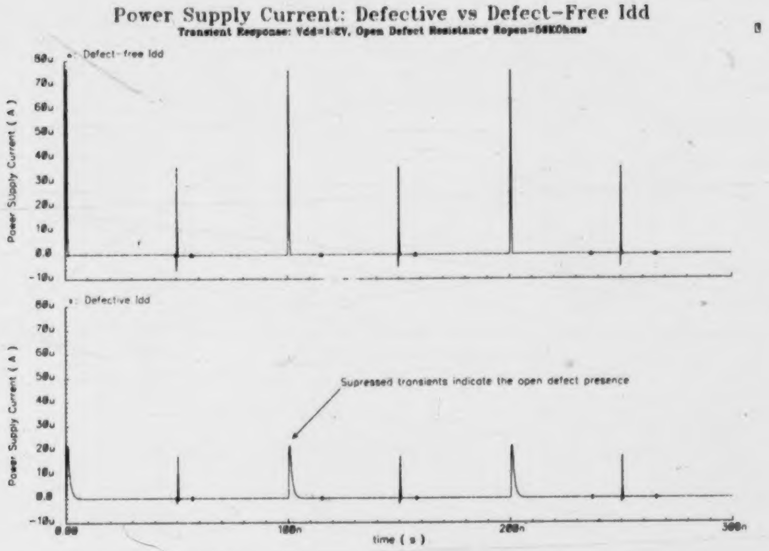

Figure 3.5: Faulty and fault-free I_{DD} current of simple CMOS inverter in the presence of the 50 Ω open defect – suppressed transients indicate open defect

been proven that some defects, such as opens, do not significantly affect quiescent current and cannot be effectively detected by I_{DDQ} test. Nevertheless, these types of defects affect a transient and frequency response of the circuit and could be detected by the I_{DDT} testing [51], [221], [167], [121]. Consequently, I_{DDT} can be used as a powerful complementary technique.

I_{DDT} testing is based on the observation that a proper working circuit draws a lot of current at the moment when it changes from one state to another. This part of the supply current is called the switching or transient current. Using the switching or transient current as the source of information to differentiate between good and defective circuits has only recently been the subject of various research activities. I_{DDT} measurements are done when the circuit under test is active, opposite to the I_{DDQ} approach, where the measurement is taking place when the circuit is in a quiescent or stable state.

The problem of extracting useful information from fast switching transient currents has been a main impediment in the development of reliable I_{DDT} test methods. The I_{DDT} decision criterion is based on the observation of two parameters: the peak value of the transient current, and the shape and duration of the transient pulse [66], [143]. Figure 3.5 displays power supply currents of the simple 0.13 μm CMOS inverter with and without open defect. Suppressed transients clearly indicate the presence of the open defect in the circuit.

Manufacturing defects affecting the functionality, timing parameters, or the circuit operation are also influencing the transient current of the circuit. The peak value of the transient current is related to the amount of switching activity that has taken place and the timeframe in which this activity happens. The fact that under certain conditions the peak value is higher than expected (more activity than expected) or is lower than expected (less activity than expected) might indicate the presence of a manufacturing defect in the circuit. Alternatively, the same applies for the charge involved in the switching action. Charge measurements can be done by integrating the I_{DDT} over a specific time interval. When activated, manufacturing defects will cause more or less charge to be involved in the switching action. Defects producing delay faults cause current (charge) to flow over a longer period of time. Therefore, a charge measurement, where charge is measured during a predefined period, is an alternative for delay testing.

The quality of a dynamic current test is degraded by normal process variations which cause the current consumed by a fault-free circuit to vary substantially [72]. It has been reported that the impact of process variations can be markedly reduced and the fault coverage improved using the energy consumption ratio (ECR) test metric, which is based on the average dynamic current consumption of a circuit [71].

Another alternative dynamic current-based method for fault detection and localization using wavelet transform based I_{DD} waveform analysis has been proposed in [14], [128]. The authors claim that the time-frequency resolution property of wavelet transform helps detect and localize faults in digital CMOS circuits.

3.3.3 Power Supply Current Test of Digital Circuits

The power supply current monitoring technique is now a well established structural test method for digital CMOS circuits. Many studies showed that some potential defects in digital CMOS devices could be detected only by applying current-based test. Also, the supply current measurements provided a way to detect other faults more easily then functional test. The research revealed that current-based methods have been very efficient in detecting majority of defects causing functional or timing failures in digital circuits [53]. Also, it has been shown that I_{DDQ} testing can be a suitable technique to replace or complement burn-in testing and that, in combination with voltage stress, it could be a very efficient quality and reliability screening technique [77]. Other studies indicated that the I_{DDQ}-only failures were likely candidates for early life time failures and field returns [45].

Detection of defects in integrated circuits assumes excitation and propagation of the defective behavior to an output. Therefore, any test approach must satisfy both excitation and propagation requirements. Achieving these requirements is difficult for voltage-based test methods. On the other hand, current-based test uses power supply lines for observation, so there are no special propagation requirements. Since power supply lines generally offer unhindered observability, test generation effort involves only excitation of possible defect sites.

Another factor affecting the test application time is the level of parallelism, that is, the number of cores the tester can handle simultaneously. Parallelism can be also be thought of in the context of the parallel propagation of the faulty behavior to the same output. Practically, one set of input test patterns can probe numerous gates for various defects, all of which will manifest themselves in the change of only one parameter - power supply current. Given the high test parallelism associated with supply current testing, there is a reduction in the test effort required to achieve a certain quality level, when using supply current measurements in comparison to traditional voltage based screening.

Table 3.1: Projected Performance-Oriented IC I_{DDQ} Values (Source: The International Technology Roadmap for Semiconductors, Semiconductor Industry Association, 2003)

Year	Maximum I_{DDQ}
2001	30-70 mA
2003	70-150 mA
2005	150-400 mA
2008	400-1600 mA
2011	1.6-8A
2014	8-20A

Table 3.1 shows expected I_{DDQ} current values for high performance integrated circuits in future technologies. These values should not used as a precise reference; rather they are meant to provide relative values as technology scales. These numbers may be several orders of magnitude lower for low-power devices. The ranges are derived from the maximum device I_{OFF}, transistor counts, typical W/L ratios, and assuming a percentage of off transistors [182].

3.3.4 Power Supply Current Test of Analog Circuits

Inspired by the success of current-based screening of defects in digital circuits, researchers tried to evaluate the applicability of the I_{DD} monitoring technique for testing analog and mixed-signal circuits. The idea was to apply, with certain restrictions, the same principle of digital circuit current-based test to analog circuits [185]. Nevertheless, the huge success in current monitoring for digital circuit has not produced the same results in the testing of analog circuits. On the contrary, many attempts to apply similar approach to detect defects in analog circuits have failed to produce strong and reliable alternative to the existing specification based analog testing. Due to the nature of analog devices, applying power supply current testing to analog circuits has been a challenging task [34].

Analog circuits have complex relations between input and output signals. Tests for analog circuits are generated directly from the circuit specifications, without reference to an analog fault model. With a large number of specifications, testing has become exceedingly expensive and time consuming. An even more difficult situation occurs when testing highly integrated analog devices. Today system-on-chip devices provide a level of integration far beyond traditional mixed-signal circuits. The observability and accessability of internal nodes is significantly reduced, and functional testing of analog devices in such environment is becoming very difficult [27].

As a result, researchers have attempted to develop a structural, model-oriented test method for analog circuits which would ease the difficulties, and enable realistic and efficient test application. A number of current-based test methods have been proposed for analog circuits. Wang *et al.* used the spectrum of the power supply current to construct the statistical signature and detect catastrophic bridge or open faults in the circuit [213]. Similarly, Camplin *et al.* observed the correlation between changes in the power supply current due to the catastrophic faults [19]. Lindermeir *et al.* considered more subtle parametric faults as well as manufacturing process and measurement noise in order to achieve more robust test design [101]. The authors chose a trapezoid input signal rich in harmonics in order to better stimulate and expose defective circuits. Another method for analog circuit based on current monitoring named I_{CCQ} has been proposed by Lammeren *et al.* [206]. Sidiropulos *et al.* proposed a DFT scheme, aimed at fully differential analog circuits, that combines two test techniques – differential power supply current ΔI_{DD} monitoring and differential output current ΔI_{OUT} checking, in a single analog self-test [185]. Fault detection is provided by means of differential measurements of the on-chip parameters, such as the ΔI_{DD} and ΔI_{OUT} currents. Due to the differential nature of the test principle used, no reference measurement is required prior to the test, thus the fault detection exhibits a significantly reduced dependency on process parameter variations, variation of temperature during the test as well as outside interferences [185]. An attempt to validate the implementation and the application of an I_{DD}-based test methodology to analog circuit in a real life ATE production test environment has been done by Manhave *et al.* in [112].

So far, many obstacles have prevented the successful application of the current-based test technique in the analog domain. A large variety of analog circuits, each with their own specifications and behavior, makes it difficult to generalize tests. In deeply embedded environments, the precision of the on-chip generation of such input signals as well as limitation in detection of parametric faults [169] reduce fault coverage. Noticeable drawbacks in some of the methods is lack of consideration for process tolerances, which undoubtedly plays an important role in threshold setting and, as a result, impairs accurate fail/pass decision. Moreover, consideration of the limited fault set, such as catastrophic opens and bridges, doesn't reflect realistic test environment.

Verification and validation[4] of analog circuits is up to now mainly done by using functional, specification-based criteria. This is opposed to the digital world where circuit functionality is generally verified during the design simulation phases, and the final wafer tests concentrate on covering set of modeled faults as well as verifying the characteristics of the fabricated circuit.

Although previous research indicated that current-based test for analog and mixed signal designs may have similar advantages as I_{DDQ} test for digital CMOS circuits, the method has not found practical implementation in the industry. Since the supply current is a general parameter for all devices, the use of supply current testing was considered as a first step towards the development of a structural test technique, applicable for both analog and mixed signal circuits.

Most of the power supply current is composed of currents from MOSFET devices in different branches of the IC circuit. Understanding the physics behind MOSFET current and its components is a requirement for developing an effective current-based test methodology. In the following section, we describe MOSFET leakage mechanisms, some of which have a major impact on the level of power supply current.

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[4] One interpretation of the difference between *verification* and *validation* is that validation ensures it is the right design, while verification ensures that the design is right. In other words, validation ensures that a design meets customer's requirements, whereas verification tests a design against its specifications.

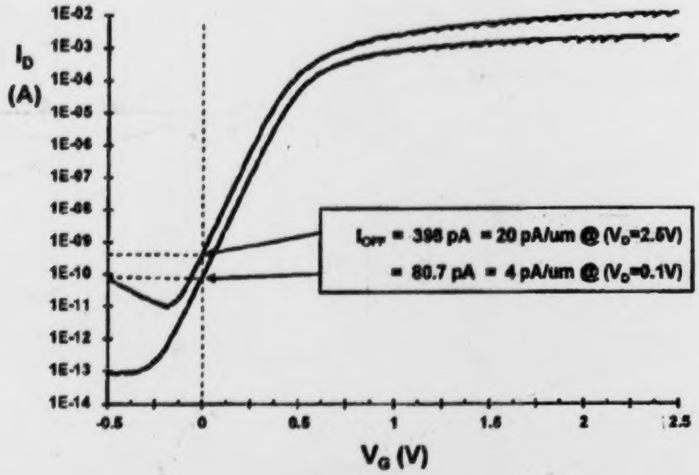

Figure 3.6: Saturated and linear MOSFET $log(I_D)$ vs. V_G characteristics [80]

3.4 MOSFET Device Leakage Mechanisms

The scientific community has invested a lot of effort investigating the dominant sources of MOSFET's leakage current [28]. The motivation is to understand the leakage properties of deep sub-micron transistors that are, beside design and performance related issues, also essential to guide effective solutions for current-based testing which relies on the accurate measurements of leakage currents.

MOSFET's off-state leakage current, I_{OFF}, is defined as drain current when the gate-to-source voltage, V_{GS}, is equal to zero. The simplified MOS transistor theory assumes a zero drain current, $I_D = 0$, for $V_{GS} < V_{TH}$. In reality, the drain current I_D does not drop abruptly, but decreases exponentially. This is shown in Figure 3.6, which plots the n-channel MOSFET characteristics $log(I_D)$ vs. V_G for linear, $V_D = 0.1\ V$, and saturated, $V_D = 2.5\ V$, mode of operation.

The leakage current is influenced by many factors such as channel length, width, threshold voltage, gate oxide thickness, drain and source junction depth, channel and surface doping profile, power supply, temperature, *etc.*. In long channel devices, I_{OFF} is dominated by the leakage from drain–well and well–substrate reverse

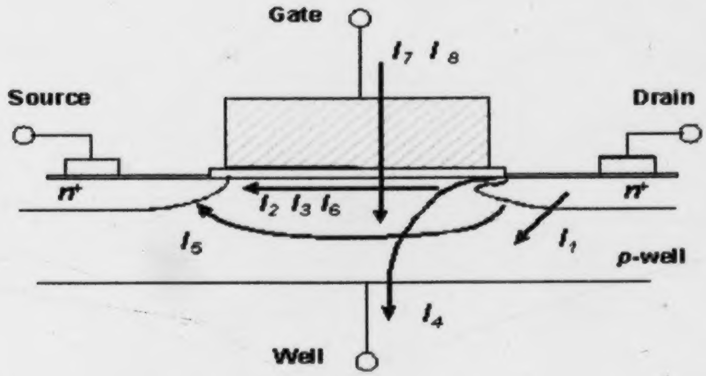

Figure 3.7: MOSFET leakage current mechanisms in DSM environment [80]

bias p-n junctions [156]. Short channel transistors require a lower power supply voltage to reduce internal electric fields and power consumption. This, in turn, necessitates a reduction of the threshold voltage V_{TH} that causes an exponential increase in I_{OFF}. This increase is due to the weak inversion state leakage that is a function of V_{TH} and not of the transistor channel length [83], [80].

In the following paragraphs, we introduce the most dominant leakage mechanisms and emphasize potential ways for their reduction. Keshavarzi *et al.* in [80] summarized eight leakage mechanisms, which are shown in Figure 3.7. These leakage components, collectively referred to as *short channel effects* (SCE), are described in the following paragraphs.

3.4.1 p-n Junction Reverse Bias Current (I_1)

Reverse biased p-n junction leakage currents are due to various mechanisms, such as diffusion and the drift of thermally generated minority carriers which are swept by the electric field in the depletion region of the p-n junctions [171]. The leakage currents of the reverse-biased source and drain junctions are state-dependent, while the leakage current of reverse-biased well–substrate junction is state-independent. If both n-type and p-type regions are heavily doped, Zener breakdown or *band-to-*

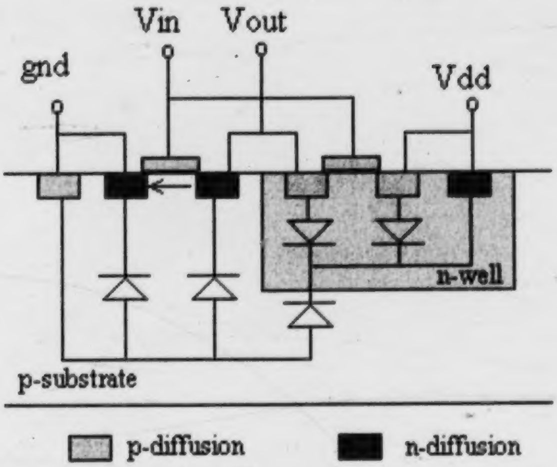

Figure 3.8: Parasitic p-n junctions in a MOSFET device with p-substrate

band tunneling[5] may also occur. The parasitic p-n junctions in a MOSFET device are shown in Figure 3.8. The reverse-bias p-n junction leakage current, I_{RB}, can be estimated by the formula

$$I_{RB} = J_s \cdot \sum_{i=1}^{n} A_i \tag{3.1}$$

where J_s denotes process defined reverse saturation current density of the p-n junction, n is the total number of reverse-biased p-n junctions, and A_i is the total area of the i^{th} junction. Since the area of the device is going to shrink, the level of this current is expected to remain unchanged or even be reduced for future technologies [166].

3.4.2 Subthreshold Conduction (I_2)

Subthreshold conduction or weak inversion current between source and drain in a MOS transistor occurs when the gate-to-source voltage, V_{GS}, is below the threshold voltage, V_{TH}. The subthreshold conduction region is seen in Figure 3.6 as the linear portion of the curve. The carriers move by diffusion along the surface similar to charge transport across the base of bipolar transistors. The exponential relation between the driving voltage on the gate and the drain current is a straight line in a semi-log plot. The subthreshold current of a MOSFET transistor can be estimated by the following formula [160],[28]:

---

[5] *Tunneling* is the quantum-mechanical process by which an electron is transported through classically-forbidden energy barriers.

$$I_{subth} = \mu_0 C_{ox} \frac{W}{L}(n-1) V_t^2 e^{(V_{GS}-V_{TH})/nV_t} \cdot (1 - e^{-V_{DS}/nV_t}) \tag{3.2}$$

where

$$n \approx 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \tag{3.3}$$

and μ_0 is the electron mobility, C_{ox} is the gate oxide capacitance, W and L are length and width of the device, $V_t = \frac{kT}{q}$ is the thermal voltage, n is the subthreshold swing coefficient (also called body effect coefficient), W_{dm} is the maximum depletion layer width, t_{ox} is the gate oxide thickness, and C_{dm} is the capacitance of the depletion layer.

The inverse of the slope of the $log_{10}(I_D)$ vs. V_{GS} characteristic is called the subthreshold slope S_{subth} and is given by

$$S_{subth} = \left(\frac{d(log_{10} I_D)}{dV_{GS}}\right)^{-1} = 2.3\frac{nkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \tag{3.4}$$

Typically, the subthreshold slope S_{subth} is around 80mV/decade at room temperature, which means that 80 mV decrease in the threshold voltage, V_{TH}, results in a 10-fold increase of the subthreshold leakage current. This slope is a function of the gate oxide thickness and the surface doping adjust implants. With the rapid shrinkage of device sizes, several second-order effects take place and, in reality, the slope becomes a function of many parameters, such as the effective channel length L_{eff}, the drain voltage V_{DS}, the body bias V_{SB}, *etc.* [198]. A slope of more than 100mV/decade is an indication that the device technology is leaky and unsuitable for high volume manufacturing. Lower values indicate a better control of short channel effect and lower I_{subth} for a given threshold voltage. The slope has not increased as the technologies advance, mainly because the thickness of the oxide has been scaled too, and the substrate doping profiles have improved [80]. Nevertheless, with advances in technology, further scaling will require reductions in the power supply voltage. A lower power supply voltage requires a lower V_{TH} which in turn results in a higher I_{subth}. Weak inversion typically dominates modern device off-state leakage due to the low V_{TH}.

3.4.3 Drain-Induced Barrier Lowering (I_3)

Drain-induced barrier lowering (DIBL) is the effect which manifests itself as a change of the MOSFET output conductance and the threshold voltage due to the voltage on the drain terminal. It is observed as a variation of the measured threshold voltage with a reduced gate length. The threshold variation is caused by the increased current with higher drain voltage as the applied drain voltage controls the inversion layer charge at the drain, thereby competing with the gate. DIBL causes the depletion region of the drain to interact with the source near the channel surface which lowers the source potential barrier. The source then injects carriers into the channel surface with a minimized role of the gate voltage. DIBL is more visible at higher drain voltages and for shorter effective channels lengths. Surface DIBL typically happens before the deep bulk *punchthrough* effect, which will be explained in Section 3.4.5.

Ideally, DIBL does not change the slope, but it does lower the threshold voltage. Higher surface and channel doping and shallow source/drain junction depths reduce the DIBL leakage current mechanism. Figure 3.9 illustrates the DIBL effect as it moves the curve up and to the left as the drain voltage increases. DIBL can be measured at constant V_G as the change in I_D for a change in V_D. This effect occurs in devices where only the gate length is reduced without properly scaling the other dimensions. This effect can typically be eliminated by properly scaling the drain and source depths while increasing the substrate doping density [201].

3.4.4 Gate-Induced Drain Leakage (I_4)

Gate-induced drain leakage (GIDL) is a parasitic current from the drain due to the high electric field located in the small area where the gate overlaps the drain. The electric field in this region is the greatest when the gate voltage, V_G, is low and

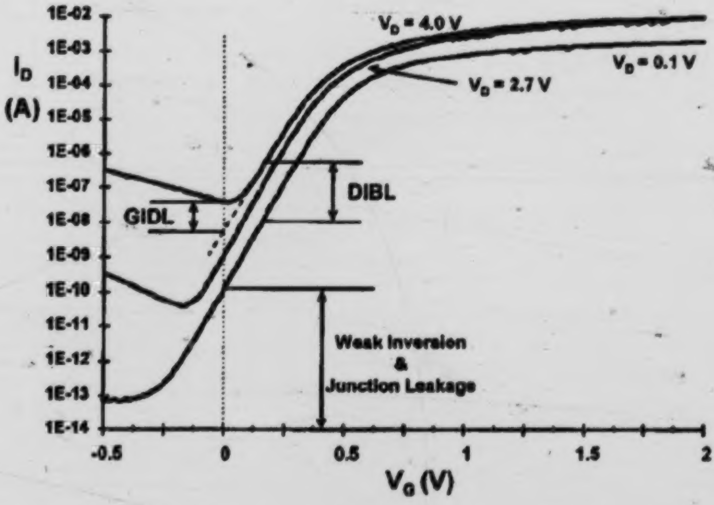

Figure 3.9: N-type MOSFET I_D vs. V_G showing DIBL, GIDL, weak inversion, and p-n junction reverse bias leakage components [80]

transistor is off. As the drain voltage is reduced, a lower voltage on the gate of the transistor is needed to produce a GIDL effect. The magnitude of the GIDL current is proportional to the width of the device. The greater the width of the transistor, the more area is covered by the gate/drain overlap, and the greater is the GIDL current. A band-to-band tunneling mechanism has been identified as a major contributor to GIDL [174], [22]. Interestingly enough, Nathan *et al.* in [130] stated quite the opposite. The authors claimed that interface trap assisted tunneling mechanisms dominate the GIDL current and that band-to-band, direct and indirect, tunneling contributions are negligible.

The electric field must exceed a critical value for the band-to-band tunneling to occur. This field results from a large positive V_{DG} voltage which forms a strong depletion region under the drain-to-gate overlap region. The presence of a gate-induced high electric field results in the emission of minority carriers which transfer by band-to-band tunneling from the valence band to the conduction band of silicon. The electrons emitted at the surface of the deep depletion layer are collected by the drain and move toward the substrate, under the transversal electric field effect. The field in silicon at the Si-SiO_2 interface depends on the doping concentration in the diffusion region and potential difference between gate and drain terminals [174].

Figure 3.9 shows increasing GIDL current for negative values of V_G. The GIDL contribution is small at 2.7 V, but it increases as the drain voltage rises to 4V. With a thinner gate oxide and higher power supply, the electric field dependent GIDL is more visible. The impact of drain and well doping on GIDL is rather complicated. At low drain doping values, there is insufficient electric field for tunneling to occur. For very high drain doping, the depletion volume for tunneling will be limited. Hence, GIDL is worse for drain doping values in between the above extremes. Very high and abrupt drain doping is preferred for minimizing GIDL as it provides lower series resistance required for high transistor drive current [80].

3.4.5 Punchthrough (I_5)

Punchthrough in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate becomes strongly dependent on the V_{DS} voltage, as is the drain current. Punchthrough causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

Punchthrough occurs when the drain and source depletion region approach each other and electrically connect deep in the channel. Punchthrough is a space-charge condition that allows channel current to exist deep in the sub-gate region causing the gate to lose control of the sub-gate channel region. Punchthrough current varies quadratically with the drain voltage and increases reflecting the increase in drain leakage. This effect is regarded as a sub-surface version of DIBL [80].

In the bulk, the incremental drain bias increases the width of the drain depletion region and the maximum lateral electric field. However, the minority carrier injection can occur only when the source barrier is lowered after the drain/source depletion regions connect. On the other hand, at the surface, lowering of the source

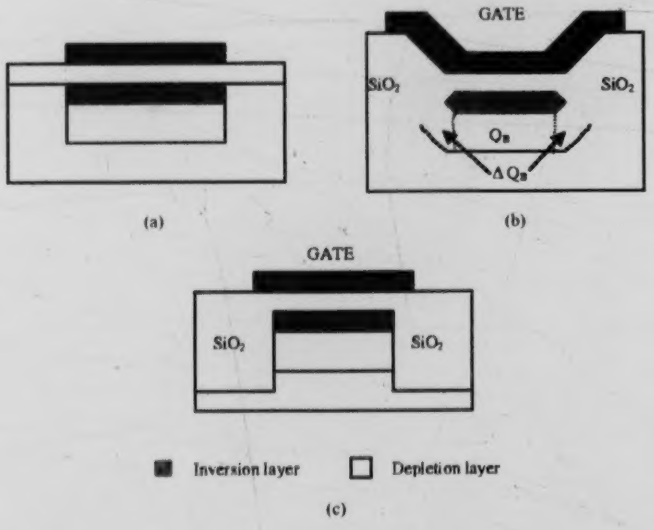

Figure 3.10: Three types of device structures and associated inversion/depletion layer: (a) Large-geometry MOSFET, (b) LOCOS gate MOSFET, (c) Trench-isolated MOSFET [30]

barrier is possible due to the extension of the lateral field toward the source junction through the gate induced surface depletion region. This effect is enhanced by a shorter physical dimension between the source and drain, and lower bulk doping concentration [42].

The most effective method for controlling punchthrough is to use additional implants. A layer of higher doping at a depth equal to that of the bottom of the junction depletion regions is one possible solution. Another approach could be to form a halo implant at the leading edges of the drain and source junctions [160].

3.4.6 Narrow Width Effect (I_6)

A decrease in the gate width affects the threshold voltage of a transistor, and, as a result, influence the subthreshold leakage. Three narrow width effects which modulate the threshold voltage V_{TH} have been identified below.

In the local oxide isolation (LOCOS) gate MOSFET, the existence of the fringing field causes the gate-induced depletion region to spread outside the defined channel width and under the isolations as shown in Figure 3.10 (b). The total depletion charge in the bulk region increases above its nominal value. The threshold voltage of MOS can be defined using the depletion approximation as in [30]

$$V_{TH} = V_{fb} + \phi_s + \frac{Q_B}{C_{ox}} \tag{3.5}$$

where V_{fb} is the flat-band voltage, ϕ_s is the surface potential, C_{ox} is the gate oxide capacitance, and Q_B is the depletion charge in the bulk. Due to the narrow-width effect, Q_B increases by ΔQ_B as shown in Figure 3.10 (b). This effect becomes more significant as the channel width decreases, and the depletion region underneath the fringing field is comparable to the classical depletion formed by the vertical field. This results in increase of threshold voltage due to narrow-channel effect. It has been shown in [40] that this narrow-width effect can be modeled as an increase in V_{TH} by the amount given by

$$V_{NCE} = \frac{\pi q N_{sub} {x_{d,max}}^2}{2 C_{ox} W_{eff}} = 3\pi \frac{t_{ox}}{W_{eff}} \phi_s \tag{3.6}$$

where N_{sub} is the substrate doping, $x_{d,max}$ is the maximum vertical depletion width, C_{ox} is the capacitance across the oxide, W_{eff} is the effective width, t_{ox} is the oxide thickness, and ϕ_s is the surface potential

The second way that narrow-width modulates the threshold voltage is due to the fact that the channel doping is higher along the width dimension in LOCOS gates. Due to the channel stop, dopants encroach under the gate. Hence, a higher voltage is needed to completely invert the channel.

A more complex effect is seen in trench isolation devices, known as inverse-narrow-width effect. In the case of trench isolation devices, Figure 3.10 (c), the depletion layer cannot spread under the oxide isolation. Hence, the total depletion charge in the bulk, Q_B, does not increase (*i.e.*, $\Delta Q_B \approx 0$), which eliminates the increase in the threshold voltage. However, due to the two-dimensional (2-D) field-induced edge fringing effect at the gate edge, formation of an inversion layer at the edges occurs at a lower voltage than the voltage required at the center. Moreover, the overall gate capacitance, C_T, now includes the sidewall capacitance C_F due to

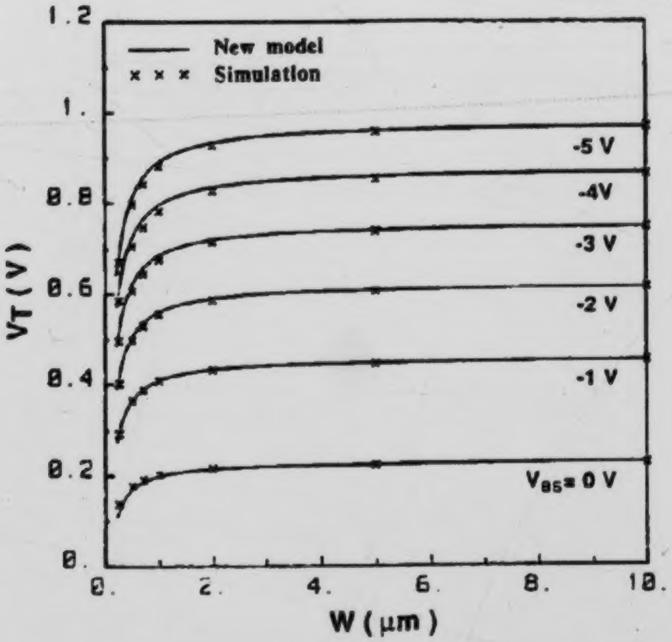

Figure 3.11: Variation of threshold voltage with gate width for uniform doping [30]

overlap of the gate with the isolation oxide. This increases the overall gate capacitance [30]. Now, the overall gate capacitance is given by $C_T = C_{ox}W + 2C_F$, which is greater than C_{ox} used in Eq. 3.5. Therefore, as shown in Figure 3.11, the overall V_{TH} is reduced.

3.4.7 Gate Oxide Tunneling (I_7)

As the gate oxide thickness of the MOSFET device scales down to only few nanometers, a substantial increase in gate leakage current is observed. The high electric field coupled with low oxide thickness results in tunneling of electrons between MOSFET substrate and gate through the gate oxide. Excessive gate leakage may affect circuit performance, functionality, and power consumption. Further reduction of oxide thickness and increased tunneling gate current may also affect dielectric integrity and reliability.

The typical leakage current of SiO_2, at a gate bias of 1 V, changes from 10^{-7} A/cm^2 at 30 Å to approximately 10 A/cm^2 at 15 Å [23]. For use in deep sub-micron CMOS technologies, the leakage current of the gate dielectric has to be kept below 10^{-8} A/cm^2. To avoid high leakage currents and still achieve the required capacitance, a material with higher permittivity should be used.

Gate dielectrics with higher relative permittivities achieve significant suppression of gate leakage. As a result, there is a significant interest in alternatives to SiO_2. The traditional SiO_2 gate dielectric will reach a fundamental leakage limit for an effective electrical thickness below 10-20Å [23]. To enable MOS scaling in the future, solutions will have to be found and technologies will have to be altered. The technology roadmap predicts the replacement of (modified) silicon dioxide dielectric by an alternative high-K dielectric material in a few years [29], [182]. The ideal solution to reduce the gate leakage current would be simply replacing the SiO_2 layer with a different dielectric material, manufactured in an equally complex process step. Unfortunately, no material which significantly reduce gate leakage current is as convenient as silicon dioxide for manufacturing.

Oxide/nitride and oxynitride gate dielectrics have been proposed to be the attractive alternatives to replace ultrathin gate oxides due to the reduction of direct tunneling current. Selective incorporation of nitrogen atoms into ultra-thin gate dielectrics improves dielectric's reliability as well as performance [177].

Figure 3.12 illustrates various gate tunneling components in a MOSFET device: the gate-to-channel current, I_{gc}, and the edge direct tunneling currents (I_{gso} and I_{gdo}) are shown. In long-channel devices, I_{gso} and I_{gdo} are less important than because the gate overlap length is small compared to the channel length. In very short channel devices, the portion of the gate overlap compared to the total gate length becomes larger and the effect of the edge tunneling currents become more significant. In ultrashort-channel MOSFETs, the source and drain extensions (overlap regions) under the polysilicon gate represent a significant fraction of the device as they do not scale at the same rate as the gate length. Therefore, the physics-based description of the overlap regions is critical for state-of-the-art MOSFETs.

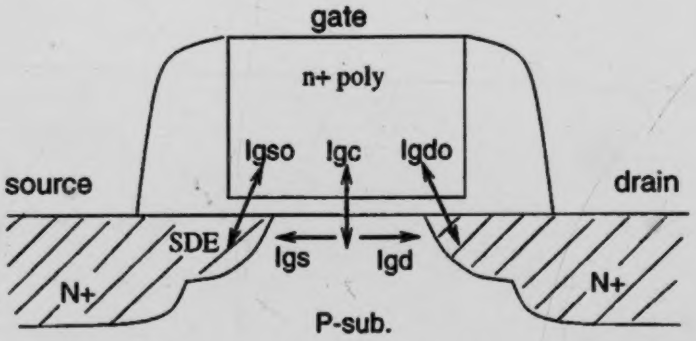

Figure 3.12: Illustration of gate direct tunneling components of a very short-channel N-type MOSFET [29]

Two models of tunneling mechanisms between substrate and gate oxide have been identified for deep-submicron devices: less dominant, *Fowler-Nordheim tunneling*[6] (FN) when electrons tunnel into the conduction band of the oxide layer, and more pronounced *direct tunneling* which happens in very thin oxide layers (less than 3–4 nm) when electrons from the inverted silicon surface, instead of tunneling into the conduction band of SiO_2, directly tunnel to the gate through the forbidden energy gap of the SiO_2 layer [160].

Gate direct tunneling current is produced by the quantum-mechanical effect of a charged carrier through the gate oxide potential barrier into the gate, which depends not only on the device structure but also the bias conditions [29]. The tunneling probability of an electron depends on the thickness of the barrier (dielectric thickness), the barrier height (electric field), and the structure of the barrier (dielectric properties). Oxide tunneling current is presently not an issue for devices in production, but could surpass weak inversion and DIBL as a dominant leakage mechanism in the future as oxides get thinner.

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[6] For devices with thick oxides, *Fowler-Nordheim tunneling* is the dominant gate current mechanism.

3.4.8 Hot Carrier Injection (I_8)

The hot carrier injection (HCI) effect can be seen in short-channel transistors which are more susceptible to the injection of hot carriers (holes and electrons) into the oxide. These charges pose a reliability risk and are measurable as gate and substrate currents. While past and present process technologies have successfully controlled this leakage component, HCI increases in magnitude as device dimensions shrink.

Hot carrier degradation in MOSFET transistors has become a great concern for scaled devices, and when the applied drain voltage is increased, as the electric field near the drain region increases. With higher fields, carriers acquire higher energy and momentum which enables carriers to penetrate a Si–SiO_2 interface as well as the SiO_2 body, creating oxide charges, and affecting device performance. The hot carriers affect device performance in all operation regimes. Most notable and monitored are the threshold voltage shifts and transconductance degradation.

Hot carriers can damage the Si–SiO_2 interface state and can cause charge trapping in the oxide due to the high channel electric field. Carriers gain kinetic energy from the lateral electric field, and some can overcome the Si–SiO_2 barrier height and cause dielectric damage. There are two ways to cause interface state generation: one is due to recombination with trapped carriers, and the other is due to breakage of Si-H bonds by energetic carriers [220].

The results of interface traps induced by ionizing radiation (or hot electrons) include stretchout of MOSFET subthreshold characteristics and capacitor CV characteristics, threshold-voltage shifts, increased surface recombination, and reduced inversion-layer mobility. However, the atomic-scale mechanisms responsible for interface-trap formation remain of extreme interest.

It is generally believed that the interface-trap formation is the result of radiation-released protons H^+ arriving at the Si–SiO_2 interface. For a positive bias voltage, protons driven by the electric field to the Si–SiO_2 interface can remove hydrogen atoms from H-passivated *dangling bonds*[7] (D) at the Si side of the interface, and form H_2 via the simple reaction [150]:

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[7] *A dangling bond* occurs when an atom is missing a neighbor to which it would be able to bind. Such dangling bonds are defects that disrupt the flow of electrons.

$$SiH + H^+ \Rightarrow D^+ + H_2. \tag{3.7}$$

This process leaves behind positively charged dangling bonds, D^+, whose charge state is afterwards controlled by the Si surface potential.

The continuous down-scaling of MOSFET dimensions without a corresponding reduction in the supply voltage has led to ever-increasing electric fields inside the transistor. Due to the pinch-off condition, the electric field peaks in the vicinity of the substrate-drain junction at the Si-SiO_2 interface. If, depending mostly on the drain bias, the lateral electric field is sufficiently high, strong carrier heating occurs and the average electron energy rises considerably above the thermal energy of the lattice. Electrons with an energy[8] exceeding a threshold of about 1.6eV (1.5 times the Si bandgap) can create electron-hole pairs in the silicon by *impact ionization*[9]. During device operation, the holes generated by this impact ionization process lead to a measurable substrate current. Electrons with a higher energy can be injected into the gate oxide. The exact barrier strongly depends on the vertical electric field and is therefore determined by the gate bias [48].

The increased random thermal motion of carriers in the channel after HCI stress increases the channel thermal noise, which is a critical factor in most RF circuit design. In addition, HCI may also trigger a breakdown of the oxide. HCI may change the device parameters which consequently affects the circuit performance. The HCI induced device degradations are correlated to the substrate current and the gate current for n-type and p-type MOSFETs, respectively. For n-type MOSFETs, the correlation exists because hot carriers are driven by the maximum channel electric field, which occurs at the drain end of the channel. For p-type MOSFETs, the charge trapping in the gate oxide is the dominant driving force for degradation, so the degradation is correlated with the gate current.

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[8] The energy of atomic particles is usually expressed in electronvolts. An electronvolt, eV, is the amount of energy needed to move a single electron through an electrostatic potential difference of one volt: $1eV = 1.6021765310^{-19}J$.

[9] *Impact (or electron) ionization* is generation of electron-hole pairs in semiconductor when high kinetic energy electrons collide with atoms in a lattice. A role and a model of the impact ionization current is described in [46].

One way to reduce the HCI effects during design is to use a cascode structure. Since HCI is caused by high voltage drop between the drain and source of the transistors, the HCI effect is reduced if V_{DS} is decreased. The cascode structure could reduce V_{DS} of the active transistor [220].

3.5 Survey of Current-Based Test Methods

Although the efficiency of traditional current-based methods has significantly decreased due to elevated leakage currents in very deep sub-micron (VDSM) technologies [215], a multitude of techniques have been proposed to improve the detection capabilities of current-based test. Some of these techniques are: I_{CCQ} power supply resistive drop monitoring [206], techniques which cope with increased leakage currents such as reverse body-bias I_{DDQ} (RBB) [25], [81], I_{DDQ} with lower test temperatures [81], divide-and-conquer I_{DDQ} test which assumes partitioning of the CUT [151]. In addition, resolution enhancement methods have been proposed such as current clustering [68], [149], neighbor selection for variance reduction [33], and wafer-level spatial correlation [163].

Among the numerous proposed current-based test techniques, the ones which attracted significant attention are undoubtedly current signatures [43], [44], current ratios [114], ΔI_{DDQ} [199], [144], and multi-parameter testing [83], [80]. Based on these methods, a number of similar or modified approaches have been proposed. The most recent comprehensive overview of the proposed current-based methodologies could be found in [164]. In the following sections, we briefly describe concepts relevant to the major contributions in this domain.

3.5.1 Single-Threshold I_{DDQ} Test

Single-threshold I_{DDQ} test is a traditional I_{DDQ} approach based on observing and measuring the current which flows when the device is in a quiescent or stable condition and comparing all measurements against a predefined pass/fail threshold. This threshold is the same for all devices tested, assuming that there is a clear distinction between leakage currents and the defect current.

The I_{DDQ} pass/fail limit is determined by sampling a portion (typically several lots) of the device material and statistically setting a pass/fail I_{DDQ} limit based on mean and standard deviation (usually 3-4 standard deviations from the mean). Any device with I_{DDQ} higher than the statistically set pass/fail limit is considered an outlier and is assumed to be a defective device. Any device which measures I_{DDQ} lower than, or equal to, the statistically set pass/fail limit is considered to be defect-free.

3.5.2 Current Signatures

The current signature method was proposed by Gattiker and Maly [43], [44]. The current signature of the integrated circuit is created by ordering all the I_{DDQ} measurements by magnitude, from the smallest to the largest value. Such a plot of I_{DDQ} measurements enables observing discontinuities in the current signature curve. The current signature method relies on the premise that I_{DDQ} for an *active defect*[10] is higher (for vectors that excite it) than normal leakage. If there are no large jumps in the plot of the current signature, then the circuit is designated as non-defective. If the plot of the current signature includes any significant jumps or discontinuities, then the circuit is designated as defective.

In the case of a *passive defect*[11], this assumption is violated as defect excitation is independent of the input pattern. As a result, the current signature of a chip with a passive defect does not show any 'steps' and can be indistinguishable from the fault-free current signature. The authors conclude that a high level 'no-step' current signature indicates a current fault which is unlikely to result in functional failure.

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[10] *Active defect* involve switching nodes of the circuit. Active faults produce abnormal current only for vectors that activate them.

[11] *Passive defects* involve only non-switching nodes of the circuit. They provide a direct, static current path between V_{DD} and ground, and produce an additional constant current for all test vectors.

3.5.3 Delta I_{DDQ} Test

ΔI_{DDQ} test has been proposed by Thibeault and Miller in [199], [120]. In this methodology, differences (deltas) between measured I_{DDQ} values are obtained and compared with a referent ΔI_{DDQ} threshold value. When measuring ΔI_{DDQ}, two approaches could be distinguished. For a *successive pattern* ΔI_{DDQ} *method*, ΔI_{DDQ} is defined as:

$$\Delta I_{DDQ}(i) = I_{DDQ}(i) - I_{DDQ}(i-1) \tag{3.8}$$

where $I_{DDQ}(i)$ and $I_{DDQ}(i-1)$ are I_{DDQ} readings for the i^{th} and $(i-1)^{th}$ vectors. For a fault-free chip, intrinsic variations of I_{DDQ} cause the mean of ΔI_{DDQ} to be close to zero. Alternatively, ΔI_{DDQ} could be defined as a difference between maximum I_{DDQ} and minimum I_{DDQ} readings. This is called a *min-max* ΔI_{DDQ} *method*. In this case, ΔI_{DDQ} can be expressed as:

$$\Delta I_{DDQ} = I_{DDQ_{max}} - I_{DDQ_{min}} \tag{3.9}$$

This method assumes that at least one vector excites the defect and the defective I_{DDQ} is much higher than the fault-free I_{DDQ}. In the case of a passive defect, all readings are elevated whereas ΔI_{DDQ} remains small. Hence, this method is unable to screen chips with a passive defect. To alleviate this shortcoming, the ΔI_{DDQ} approach could be combined with a single-threshold I_{DDQ} method to improve detection of passive defects [199].

3.5.4 Current Ratios

The concept of current ratios (CR) was proposed by Maxwell *et al.* [114]. It was observed that the ratio of maximum I_{DDQ} to minimum I_{DDQ} for fault-free chips was approximately the same although their absolute I_{DDQ} values were different. The key assumption with regard to finding defects is that the test vector set is constructed so that it will cause large variations in the current produced by most possible defects. The increase in I_{DDQ}, influenced solely by the process variations, is uniform for all vectors, and therefore, doesn't impact CR. CR can be understood as a measure of allowed intra-die variability in I_{DDQ}. Through characterization, the input vectors that cause minimum and maximum I_{DDQ} are determined and CR is obtained. To account for intra-die process variation, a guard band is added.

However, even for fault-free chips, the current ratios could show variations of more than an order of magnitude. Thus, current ratios may be comparable for defective and defect-free chips. Deciding the appropriate current ratio can be challenging. As in any signature-based approach, this method does not detect passive defects which cause high I_{DDQ} on every vector, unless the current is above the absolute maximum. For such defects, the current ratio gets smaller with increasing background leakage. Although it is possible to screen such chips by setting a lower threshold on CR, the ability to sense more subtle variations with high background current significantly diminishes.

3.5.5 Multi-parameter I_{DDQ} Test

Multi-parameter I_{DDQ} test correlates circuit leakage current against other parameters such as circuits operating frequency or temperature, and may use another variable to enhance the test sensitivity. In [82], Keshavarzi *et al.* explored intrinsic dependencies of transistor and circuit leakage on clock frequency, temperature, and reverse body bias (RBB) to discriminate defective ICs. Transistor and circuit parameters were measured and correlated, and it has been shown that by using multiple parameters, it is possible to develop I_{DDQ} testing solutions with improved sensitivity. For high performance IC applications, a multi-parameter test technique is proposed, I_{DDQ} versus F_{MAX} (maximum operating frequency), in conjunction with using temperature (or RBB) to improve the defect detection sensitivity.

The roots of leakage to frequency correlation exist in device physics and for a circuit designed on a given process technology, one can establish and characterize such a relationship. Authors in [79] found a clear correlation between the I_{DDQ} and the maximum operating frequency (F_{MAX}) of a microprocessor, as both are functions of device's channel effective length, L_{eff}. The fault-free I_{DDQ}, strongly influenced by subthreshold leakage (Section 3.4.2), has an exponential relationship with temperature as described by Equation 3.4 on page 47. Faulty or defective current does not show such a relationship. The dependence of the fault-free leakage on temperature can be exploited by making current measurements at two temperatures. The defective current may remain the same or decrease (due to a positive temperature coefficient for a resistive metal short) with an increase in temperature. This makes differentiation between fault-free and faulty chips possible. Testing can be performed by measuring I_{DDQ} at room temperature and either at a reduced or higher temperature [144]. Low temperature measurement is undesirable in production due to high cost.

3.6 Limitations of Static Current-Based Test

Sufficient research supports the notion that traditional current-based test techniques will sooner or later reach their limit of effectiveness as a result of device scaling. As described in the previous sections, one of the substantially affected parameters by scaling is the leakage current. A crucial requirement of the current-based test is the ability to accurately measure a very small variation of the power supply current. The test is based on the estimation of the defect-free current in the circuit which is used to determine a maximum non-defective current, *i.e.* I_{DDQ} threshold. Multiple current measurements are taken, and if any measurement exceeds the threshold, the chip is considered defective.

Due to the many factors affecting the process variation, the distribution of the measured I_{DDQ} currents is expected to be Gaussian[12]. In order to make a correct decision, the I_{DDQ} of the fault-free device has to be at least one order of magnitude lower than the I_{DDQ} current of the faulty device. With millions of transistors implemented on a single chip, the leakage current becomes significant and, consequently, the absolute variation of the fault-free current increases, too. As a result, the values of the fault-free and faulty I_{DDQ} currents start to overlap which makes it difficult to

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[12] *Gaussian distribution* is also called *the normal distribution*. *The central limit theorem* explains why many distributions tend to be close to the normal distribution. As stated by this theorem, if the variables have a finite variance, their sum will be approximately normally distributed. Since many real processes yield distributions with finite variance, this explains the widespread application of the normal distribution.

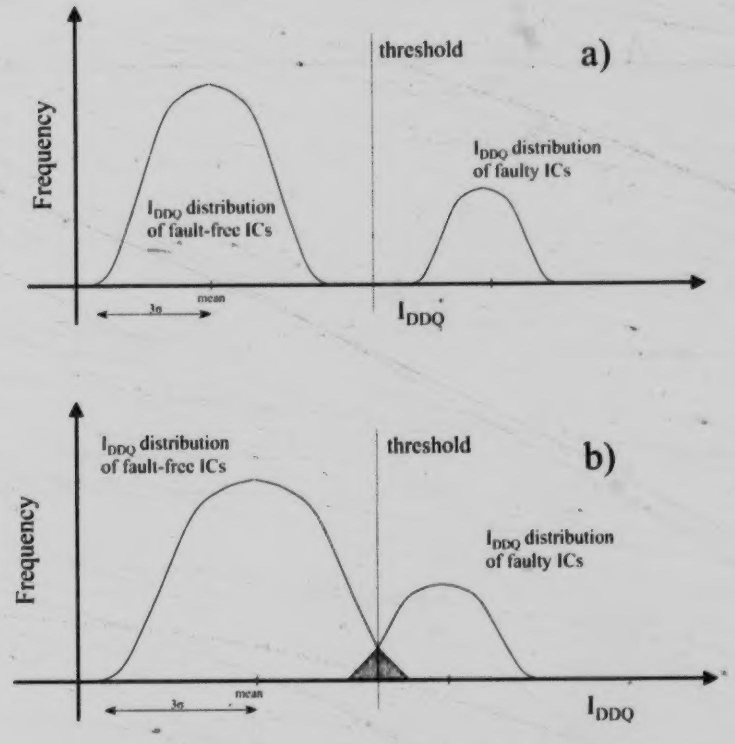

Figure 3.13: Overlapping of faulty and fault-free I_{DDQ} distributions

set a threshold value and make a reliable pass/fail decision.

Such case is illustrated in Figure 3.13. When the density functions of the defect-free and defective currents are distanced from each other, the clear distinction between the good and the defective IC can be made, Figure 3.13 (a). Nevertheless, the technology scales down device dimensions and increases a number of devices on the chip. As a result, the mean values of the defect-free and defective distributions tend to get closer to each other, eventually resulting in partially overlapped distribution and a hardly identifiable I_{DDQ} threshold [215]. Such a case is illustrated in Figure 3.13 (b).

To understand this, lets assume that a simple defect-free circuit in 0.18 μm technology contains a chain of 100 inverters operating at 1.8 V power supply and nominally consumes 500 nA[13] of static power. Lets say that the same but defective circuit contains a gate-oxide defect in one of the inverters which effectively bridges the drain and gate of the p-type MOSFET device through the 1 MΩ resistance. The difference of potentials between two bridging nodes (drain and gate) is 1.8 V which implies that additional current of 1.8 μA will be drawn from the power supply. It is clear that 'abnormal' 2.3 μA supply current (1.8 μA + 500 nA) will be easily distinguished from the fault-free one (500 nA), even in the presence of process variations which could double or even triple the nominal power supply current.

Similarly, lets assume the same circuit in 65 nm process with the 0.8 V power supply and understandably higher nominal leakage currents (due to the lower threshold voltage and other factors) of, say, 3.5 μA[14]. The same defect would cause additional power supply current of 0.8 μA which is only around 23% of the nominal leakage. Because of the exponential dependence of leakage on process parameters (gate length, oxide thickness and threshold voltage), the process imperfections could easily cause variations of such a degree. Therefore, it would be difficult to conclude if the observed current increase is a result of process variations or presence of a defect.

Controlling process variation and leakage has become critical in designing and testing ICs. Die-to-die and intra-die parameter variations are worsening with technology scaling. Elevated transistor leakage and excessive parameter variations in scaled process technologies threaten the feasibility of leakage-based current tests. Motivated by the adverse effects due to the increased device leakage trends, researchers have invested a significant effort to develop new strategies which would reduce the leakage and extend the effectiveness of current-based testing for deep sub-micron technologies [38]. The developed methods could be grouped in the domain of process technology, circuit architecture, and test technique.

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[13] Based on the figure provided in [180] for the maximum MOSFET leakage current $I_{off} = 0.01 \frac{\mu A}{\mu m}$ at 25°C, assuming minimum device length and width of $W = 500\ nm$

[14] Based on the figure provided in [183] for the nominal high-performance 65 nm MOSFET subthreshold leakage current $I_{sd} = 0.07 \frac{\mu A}{\mu m}$ at 25°C and assuming device width of $W = 500\ nm$

Circuit techniques which reduce leakage currents during standby states and minimize power consumption such as source biasing, dual-V_{TH} partitioning, multi-threshold CMOS (MTCMOS), and variable threshold CMOS (VTCMOS) are described in [75]. In [160], authors survey several process methods (retrograde doping, halo doping) and circuit techniques (transistor stacks, multiple threshold voltages, dynamic threshold voltage, *etc.*) for leakage control and reduction.

(no text)

Chapter 4

Power Supply Current Monitoring

4.1 Introduction

Ensuring the quality of IC electronic components and systems requires effective test strategies to be applied to the circuits of increasing complexity and size. The traditional specification techniques based on the analysis of the output signals have been found insufficient and impractical to guaranty the high reliability and low defect escape requirements of the ICs with growing complexity. This fact has motivated the search for complementary testing techniques which could improve existing test methods and translate them into higher product quality. In the quest for more effective test methodology, current test methods have a proven record of successful application in the industry as a complementary test technique.

The object of current-based test is the power supply current of the circuit under test. This current is sensed, measured, and analyzed for the purpose of detecting a defective device. The means by which current sensing and measurements are performed is a device called a *current monitor* (CM). Current measurement units are realized as stand-alone, off-chip external circuits or they are integrated (built-in) together with the tested circuit on a common substrate. While built-in current sensors (BICS) generally exhibit a better fault observation, off-chip monitors offer more versatility.

Monitoring current flow into and out of electronic circuits is an essential task in designer's portfolio, and is necessary in a wide range of applications including a system control, protection, and diagnostics. Besides the current-based testing, examples include over-current protection, supervising devices, programmable current sources, linear and switch-mode power supplies, battery chargers, and battery-operated circuits for which the ratio of current flow into and out of a rechargeable battery has to be known. As more applications become portable, the demand increases for dedicated current monitors that accomplish their task in a small package and with low quiescent current. The number of applications requiring current sensing is continuing to expand. Depending on the demands of an application a number of different techniques for sensing current are available.

The following sections attempt to define requirements for the current monitor designs, to outline different technologies for current sensing, to explore existing design methodologies and summarize different design concepts and principles of current sensing in I_{DD} testing applications. Also, a brief survey of the state of the art current monitor devices reported in the literature is provided.

4.2 Current Monitor Design Requirements

The majority of I_{DD} methods presented in the literature have been implemented as off-chip monitors. Also, many on-chip sensor designs have been proposed. However, very few have been included in the commercial designs for production and life-time testing. This is primarily due to the strict criteria placed upon the on-chip sensors. Rajsuman in [146] concluded that the on-chip current sensors impose design constraints which limit their use. Some of the criteria for a practical on-chip sensor have been outlined by Kim *et al.* in [84]. In the following paragraphs, we summarize the most important requirements and desirable features of the current monitor which has to be aimed for during the design process. Some of the items described below could be applicable to any current monitor, whereas the others are more specific to built-in designs.

- Performance loss of the circuit with the attached monitor has to be kept within reasonable margins (*e.g.*, less than 2-3%);

- The dynamic range of the current measurement circuit should accommodate measurements of wide range of current levels (*e.g.*, the variability of current levels for a given technology is expected to be high);
- High resolution (low noise) is required for the detection of subtle defects which cause only a micro-Ampere increase in the power supply current (*i.e.*, resolution of an analog signal is limited by noise);
- High linearity of the monitoring device is required for accurate measurements of the wide current ranges;
- No significant increase in power supply noise should occur due to the on-chip I_{DDQ} design-for-test (DFT) circuitry;
- Chip area overhead must be kept at a minimum, usually not more than few percent of the circuit under test area;
- Implementation of the sensor should not require special semiconductor processing steps (*i.e.*, cost and economic related issues);
- The monitor should be capable of relatively high speed test measurements (*e.g.*, faster than typical 1 kHz – 10 kHz off-chip current measurements);
- A monitor should be capable to measure the power supply current level, instead of providing only a pass/fail signal;
- The monitor has to fit within existing DFT standards for the purpose of controlling the on-chip circuitry;
- The monitor should be usable at wafer level but also during package test;
- On-chip DFT circuitry must have reasonable power dissipation when in use, and low or no dissipation when inactive (*e.g.*, useful reference for this is a device under test (DUT) power consumption);
- Good fault coverage throughout multiple technology nodes must be demonstrated in applications.

4.3 Current Sensing Techniques

A continuous current measurement can provide a lot of information about the device under test. The methods of supply current sensing, observation, and measurement are used in a wide variety of applications and are not limited to testing only. Current sensing methods have been extensively researched and reported in the literature [162], [140], [94], [219]. Three basic categories of current sensing techniques can be distinguished: 1) devices based on resistive sensors, 2) devices based on magnetic sensors, and 3) devices based on current transformers.

4.3.1 Sense Resistors

Sense resistors or current shunts are distinguished from resistors by the fact that they are designed for the purpose to sense and measure the current which flows through it. They are placed in series with the load. By Ohms law, the voltage drop across the device is proportional to the current. For low currents, sense resistors can provide accurate measurements provided the resistance value has a tight tolerance. Sense resistors also require other circuitry, such as instrumentation amplifiers, to generate a detectable signal. Although current shunts operate on the principle of the Ohmic voltage drop, practical shunts could have intrinsic inductance which would limit the accuracy and bandwidth. Beside this, the major factors which affect the precision of a shunt are: the temperature coefficient, power dissipation, low output signal, and insertion loss [16].

A current probe can be used in between the circuit under test and power supply, as shown in Figure 4.1. The problem with such probing is the insertion of serial inductance that is typically in the 10nH to 50nH range. When a transient current pulse of 1A/ns is fed into a 10nH inductive probe, it causes about 10 V voltage drop across it. Apparently, such probing cannot be efficiently utilized as it would severely affect circuit's performance. A design alternative is to use an operational amplifier with sufficient gain which would place the current sensing resistor in its feedback loop, as shown in Figure 4.2 (a). The op-amp should be designed to

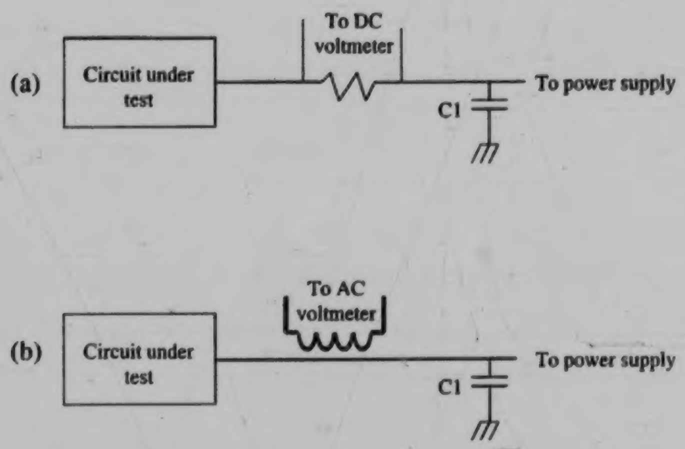

Figure 4.1: Current measurement methods: (a) DC current probe, (b) AC current probe [78]

compensate for the voltage drop across the sense resistor, and at the same time, it should be able to supply sufficient transient currents to the circuit for fast charging and discharging of capacitor states. Obviously, designing such a current sensor wouldn't be a trivial task. The solution to this problem is to provide a shunt path for the transient current across the sense resistor. If this shunt path is provided by a diode, as shown in Figure 4.2 (b), it would cause about a 0.6-0.7 V drop across it, which would make it difficult for applications in low voltage environments.

To avoid this voltage drop across the shunt path, a MOSFET bypass circuit can be employed as shown in Figure 4.2 (c). The bypass transistor is on only during the transient. When the transients are settled down, the current is passed through the sense resistor. To filter the high impedance noise at high frequencies, a small capacitor is added in between the sense circuit and the circuit under test, as shown in Figure 4.2 (d). A disadvantage of this method is a RC loading at the output, which increases the time for the circuit to arrive at a steady-state. By closely observing the circuit in Figure 4.2 (d), it can be concluded that the resistance in the sense circuit is redundant. A bypass circuit will enable flow of the transients through a small on-resistance of the forward conducting MOSFET device, R_{on}. In this way,

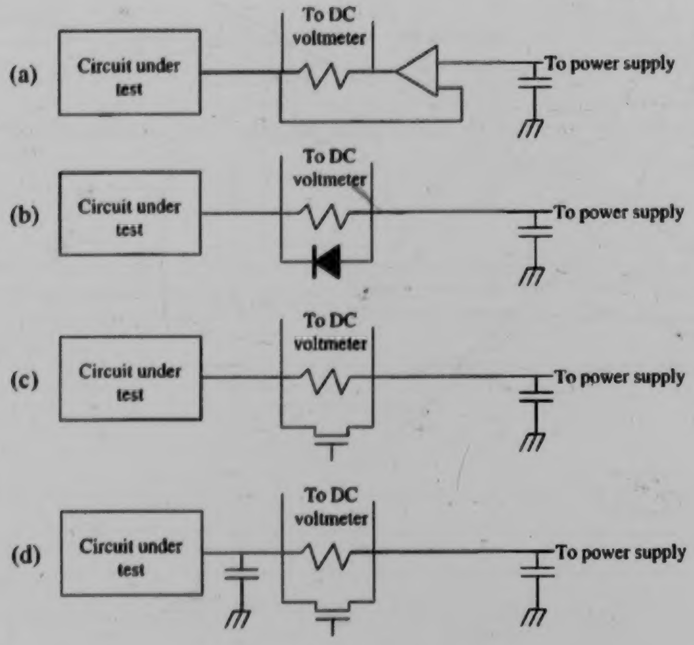
(a)
Circuit under test
To DC voltmeter
To power supply
(b)
Circuit under test
To DC voltmeter
To power supply
(c)
Circuit under test
To DC voltmeter
To power supply
(d)
Circuit under test
To DC voltmeter
To power supply

Figure 4.2: Different power supply current DC probing methods [78]

the testing speed can be further improved. This approach is shown in Figure 4.3. In this circuit, the MOSFET is on during the transient when the circuit under test is drawing a large current. Once the transients are settled, the MOSFET is off and capacitor C_1 supplies the static current to the circuit under test. The I_{DD} is measured by the voltage drop across the MOSFET. In this circuit, the value of capacitor C_1 is critical, it should be chosen such that in the fault-free circuit, it will keep V_{DD} to the specified testing voltage at-least until the measurement is done [78], [146].

A careful consideration of the sense resistor is an important and necessary part of designing any kind of current monitor. The following criteria should be taken into consideration:

Voltage loss: High resistance values cause the power and supply voltage to degrade through the voltage drop loss. The lowest resistance value gives the least voltage loss.

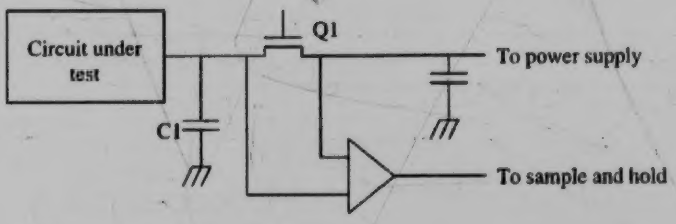

Figure 4.3: External current-sense circuit to avoid RC loading at the output [78]

Accuracy: High resistance values enable more accurate measurements and better sensitivity to low-level currents because the voltage offset and input bias-current offsets are less significant with respect to the sense voltage.

Efficiency and power dissipation: At high current levels, the power dissipation loss in the sensing resistor can be substantial, so it must be taken that into consideration when choosing the resistor value and the power dissipation rating. Excessive heat in the sense resistor can also cause its value to drift.

Inductance: If the supply current has a large high-frequency component, a sensing resistor must have low inductance. Wire-wound type resistors have the highest inductance. Low-inductance metal-film resistors, which consist of a straight band of metal, are the best choice.

Cost overhead: The sensor should be compatible with a manufacturing process. Sensing elements which requires additional manufacturing steps increase the cost and are not well suited solutions.

4.3.2 Magnetic Current Sensors

In order to reduce power supply degradation of the circuit under test, many researchers have attempted to develop non-intrusive current measurement methods. The magnetic current sensor is a typical result of such efforts. Magnetic sensors comprise devices which measure the magnetic field generated by the current flow.

When a magnetic field is applied to conducting or semiconducting material in which current is flowing, a voltage will be developed across the sides of the material. This is known as the *Hall effect*. A wide variety of semiconductor devices have been designed and investigated as magnetic field sensors such as Hall cells, magnetodiodes, magnetoresistors (MR), bipolar magnetotransistors (MT), and magnetic field-effect transistors (MAGFET) [98].

Hall cells are used for contactless measurement in many applications. However, the Hall element fabricated in CMOS IC technology has mediocre characteristics. It gives a weak output signal which is often corrupted by a sensor offset and noise [147]. Most attention attracted MT and MAGFET devices compatible with CMOS and/or bipolar silicon processes [118], [119]. The split-drain magnetic field effect transistor (MAGFET) is an attractive alternative for implementation in silicon due to its simplicity and total compatibility with standard CMOS processes. It appeared as a solution to overcome the difficulties of implementing sensitive Hall cells in silicon. Diverse configurations of split-drain transistors were proposed thereafter. Exhaustive measurements of this type of a sensor, operating in distinct conditions, have also been reported in literature.

The major factors affecting the precision of Hall effect current sensors are temperature sensitivity, noise, linearity, leakage flux sensitivity, and sensitivity to control current. Although extensively used in industrial applications [98], rarely proposed magnetic current sensors for IC current-based testing applications, such as in [85], have not proved so far to be an efficient sensing solution.

4.3.3 Transformers

Current transformers are passive devices that do not require a driving circuitry to operate. The primary AC current will generate a magnetic field that is coupled into a secondary coil by the *Faraday's law*[1]. The magnitude of the secondary current is proportional to the number of turns in the coil. The secondary current is then sensed through a sense resistor to convert the output current into voltage.

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[1] *Faraday's law* describe the relation between the rate of change of the magnetic flux, $\frac{d\Phi_B}{dt}$, through the area, **s**, enclosed by a closed loop and the electric field, **E**, induced along the loop: $\oint_S \mathbf{E} \cdot d\mathbf{s} = -\frac{d\Phi_B}{dt}$. In the case of an inductor coil where the electric wire makes N turns, the formula becomes: $V = -N\frac{\Delta\Phi}{\Delta t}$, where V denotes the induced electromotive force.

The principal advantage of using current transformers to measure current in electric circuits is that the measurement circuit can be electrically isolated from the circuit under test, as shown in Figure 4.1 (b). This non-contact approach to current measurement greatly facilitates the simultaneous measurement of current and voltage in different branches of a common circuit. Due to the non-ideality of the transformer elements, current transformers could impose a burden on the circuit under investigation if placed in the power supply line, especially in low voltage environments. Discrete transformers achieve much higher quality factor over their silicon counterparts, and, generally, their use has an insignificant effect on the performance of the circuits examined.

For the applications where AC measurements are the subject of interest, a transformer could be an effective solution. However, I_{DDQ} current-based test applications require measurements of the DC current levels for effective defect screening. Moreover, the difficulty of implementing high quality transformers in silicon makes this current sensing techniques impractical for on-chip I_{DDQ} test.

4.4 Off-Chip Current Monitoring

A widely used approach for current monitoring is off-chip current monitoring. For the purpose of test, both DC and AC current measurements are important. Many semiconductor companies perform I_{DD} testing through the external tester which contains a high accuracy precision measurement unit (PMU) [139]. PMU incorporates an electromechanical relay which switches the connection from a device power supply (DPS) to PMU to perform the current measurement. After the measurement, DPS is switched back by the relay. Each switching phase of relay requires a delay equivalent to settling time. As a result the current measurements are relatively slow.

A number of manufacturers include current measurement feature in the automatic test equipment (ATE). These additional hardware tools could perform I_{DDQ}

testing at frequencies of up to 100 kHz [146]. However, in many practical cases, the current monitoring is done at significantly lower frequencies, in the 1-20 kHz frequency range[2]. Since most IC manufacturer use only a few I_{DDQ} measurements, they use the tester's PMU instead of dedicated I_{DDQ} high-resolution test hardware in production testing. Due to the time-to-market and cost related issues, I_{DDQ} testing with a large number of vectors is not done very frequently in the production environment.

4.5 On-Chip Current Monitoring

While most of the work in mid 1980s on current measurement was based upon off-chip measurement circuitry, around 1989 proposals appeared for on-chip current sensors. In 1993, the IEEE Technical Committee on Test Technology founded the Quality Test Action Group (QTAG) task force to investigate the feasibility of a standard for I_{DDQ}/I_{SSQ} current sensors [10].

QTAG was created to provide the industry with a standard for I_{DDQ}/I_{SSQ} monitors on test fixtures for production testing of CMOS ICs. The group was founded since informal correspondence between the semiconductor test departments and the ATE vendors had failed to initiate creation of the ATE-based I_{DDQ} test instrumentation needed by the semiconductor industry. During the first QTAG meeting, the participants described the situation and proposed that the solution utilize the technology that the industry and universities had developed for on-chip I_{DDQ} testing.

Since off-chip current sensors are usually implemented by external automatic test equipment (ATE), using built-in current sensors (BICS) offers many advantages. BICS could significantly reduce the test equipment cost [60]. A high capacitance of I/O pads reduces the testing rate using ATE which makes on-chip test methods much more suitable for high frequency testing. BICS improves the detectability and observability of the circuit under test and provides higher testing resolution. Nevertheless, implementation of on-chip testing presents many challenges. Recently much work has been done in order to improve BICS sensitivity and reduction in degradation of the circuit under test (CUT) performance, as these are two important elements of the current sensor design.

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[2] For example, based on the PMU data sheet from Maxim Integrated Products (http://www.maxim-ic.com/), the PMU settling time for the current range of ± 2 μA is given as 500 μs, which corresponds to the measurement speed not exceeding 2 kHz. Similarly, a system reference manual for Agilent 93000 SOC Series tester (http://www.agilent.com/) indicates a maximum I_{DDQ} measurement speed of 3 kHz at 1nF load capacitance.

The design of a built-in current current monitor is a trade-off between circuit speed, size, sensitivity, and accuracy. The higher resistance of the sensing element leads to an increased sensitivity but also to a lower speed and a higher voltage supply degradation which is very important for low voltage designs.

4.6 Survey of Proposed Designs

A number of current monitors have been presented. A comprehensive survey of the proposed designs published in journals and major conference proceedings is given in this section. Selected twelve current monitor designs, which have been most referenced in the literature, are described here in more details. Schematics and detailed circuit operation of these twelve monitors are provided. Due to the large number of designs, other proposed circuits are only briefly described. For more specific design details, the reader is encouraged to refer to the cited publications and patents.

Alorda *et al.* presented an off-chip monitor in [3], [4] which measures the transient supply current of CMOS ICs and provides a voltage level which corresponds to the charge delivered to the circuit for each clock cycle. The monitor is designed to be placed on the automatic test equipment board fixture and automate transient current supply testing.

A 5 V BICS scheme suitable for on-line power dissipation measurements and I_{DDQ} testing has been proposed by Arabi and Kaminska in [7], [5]. The BICS, shown in Figure 4.4, has been implemented using an N-well CMOS 1.2 μm technology. The current sensor has been integrated with the voltage down converter and targets applications that require on-chip supply voltage down-conversion. Transistors P_4, P_5, and P_6 along with the operational amplifier OA_2 provide I'_{CUT} which

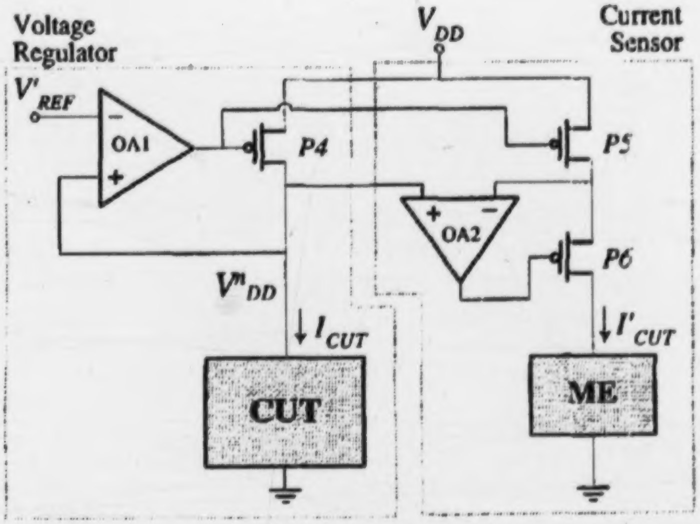

Figure 4.4: BICS proposed by Arabi and Kaminska [5]

is a scaled copy of the current passing through the circuit under test (CUT) I_{CUT} and can be measured using measurement element (ME). The V-I characteristic of transistors P_4 and P_5 when they are in the linear region is given by:

$$I_{ds} = \mu_0 C_{ox}\frac{W}{L}((V_{gs}-V_t)V_{ds}-\frac{V_{ds}^2}{2}) \approx \mu_0 C_{ox}\frac{W}{L}(V_{gs}-V_t)V_{ds} \qquad (4.1)$$

Equation 4.1 indicates that to establish the same I_{ds} current in both the P_4 and P_5 transistors, their V_{gs} and V_{ds} voltages must be equal neglecting the body bias effect. Physical connections between their gates and sources makes their V_{gs} voltages identical. The feedback established by OA_2 forces the drain voltage of transistors P_4 and P_5, and consequently their V_{ds} voltages, to be equal resulting in an accurate current sensing even when the transistor P_4 is in the linear region due to the close values of V_{DD} and V''_{DD}. The voltage drop across transistor P_4 can be as little as 0.15 V when its W/L ratio is big enough to minimize its R_{ON} resistance. Although V''_{DD} voltage levels close to V_{DD} can be achieved, the current mirror loses its accuracy when the V''_{DD} voltage level exceeds 4.25V. This is due to the input voltage limitation of the operational amplifier OA_2 which cannot approach the power supply rails. Therefore, to improve the accuracy of the current mirror, a rail-to-rail operational

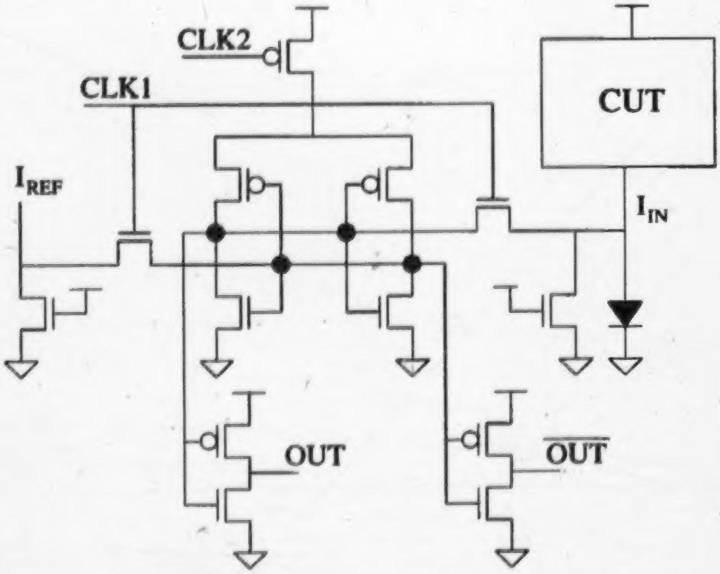

Figure 4.5: BICS proposed by Shen *et al.* [176]

amplifier should be utilized. Even with such improvements, 5 V BICS with 0.15 V reduced voltage supply of the CUT, will likely not find a suitable application for circuits with the now widely used 1-1.8 V power supply.

Shen *et al.* described an experimental 5 V CMOS chip containing a built-in current sensing circuit design shown in Figure 4.5 [176]. The chip has been implemented in a 2 μm p-well CMOS process. The authors report that BICS circuit can detect defects at a clock speed of 30 MHz. This design is based on a sense amplifier structure similar to the bit-line sense amplifier employed in dynamic memories. The BICS develops a voltage across the parallel transistor-diode combination in response to input current, I_{IN}. A sensing amplifier converts this voltage to a logic level. Two identical n-type MOSFETs are used to sample the power bus current of the functional circuit and I_{REF}, respectively. To increase the evaluating speed, a diode is used to bypass the transient power bus current of the functional circuit. This limits the voltage drop across the sensing circuit to less than 0.65 V which results in about a 10-15% decrease in the speed of 5 V CMOS circuits. Clock signals are employed to isolate the sensor amplifier from the input node during the transient state of the circuit under test (CUT), and to prevent the CUT from being affected by the signals within the current sensing circuit. To increase the sensitivity of the BICS, a two-phase non-overlapping clock signal is utilized. A major problem with this and most other designs presented so far affects the operation at high speeds. It can be observed in Figure 4.5 that, as the number of gates in the CUT is increased, the total capacitance between the current input node of the BICS (the virtual ground node of the CUT) and (true) ground increases proportionally. This includes the capacitance of the metal circuit ground net and the parasitic capacitances associated with the source diffusion regions of transistors connected to the circuit ground. For circuit partitions of even modest complexity, this capacitance across the diode can easily be in the picofarad range. A design based on Shen's design with reduced area overhead and increased fault detectability has been proposed by Athan *et al.* in [9].

Burgess [17] proposed a differentially configured built-in current sensor which monitors a V_{DD} line. The regeneration time of the cross coupled latch of the sensor is proposed as a defect metric. The author reports speed and functionality enhancements over previous BICS designs. The BICS fits within the QTAG standard for off-chip current sensors either as a threshold or measurement monitor.

In [37], Favalli *et al.* demonstrated several design oriented approaches to improve design for testability (DFT) of CMOS digital circuits. The design, shown in Figure 4.6, detects delay and non-stuck-at analog faults which cause intermediate voltages along circuit branches due to faulty conductive paths between the power supply and ground. CMOS gates are modified with the insertion (between ground and the n-channel networks) of n-channel MOSFETs (M_T) whose drains (nodes N_{low}) represent the inputs of a NOR gate realized with n-channel drivers, M_{TD}, and a p-channel pull-up device, M_{TL}. In normal mode, the control line t is at logic one, so all M_T transistors are on, while M_{TL} is off. In test mode, the command signal t is first set to one, and suitable test patterns are applied to activate the possible faults; successively t is switched to zero. If no fault is present, no conducting path is established between the power supply and the nodes N_{low} which consequently remain

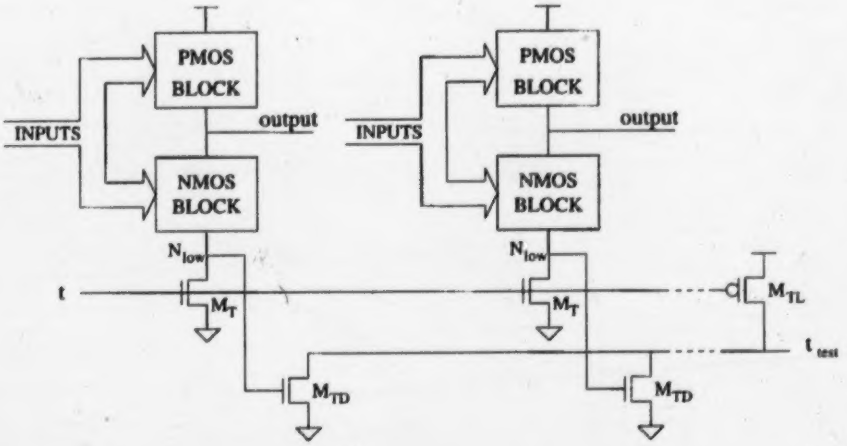

Figure 4.6: BICS proposed by Favalli *et al.* [37]

at logic zero. Hence, all the drivers of the test NOR are off, and t_{test} is high. On the contrary, in the case of a fault establishing a connecting path through the pull-down and pull-up networks of the CMOS circuit, N_{low} can be charged to a high value, thus M_{TD} becomes conducting, and t_{test} is lowered to logic zero.

In [61], Hsue and Lin described a 5 V CMOS current sensor circuit using a diode as a sensor which can be built into a CMOS logic circuit to perform a self test for leakage current.

A differential 5 V design implemented in 2 μm technology, shown in Figure 4.7, was presented by Hurst and Singh in [62]. This BICS design attempts to reduce a critical capacitive time-constant problem of Shen's design from Figure 4.5 by using a similar differential sensor. In this sensor, the two input nodes of the latch could be connected to separate partitions of the CUT. Or alternatively, reference current is activated on only one side of the latch at a time, while the circuit attached to the other side is being tested. The sensor design also includes an NPN bipolar transistor in parallel with the diode to minimize supply voltage drop during normal (no-test) operation. A standard two-phase non-overlapping clock is required for timing of the sensor. When testing the circuit, transistors T_1 and T_2 are turned off by grounding $TEST$, and a reference current is provided by grounding the appropriate REF node.

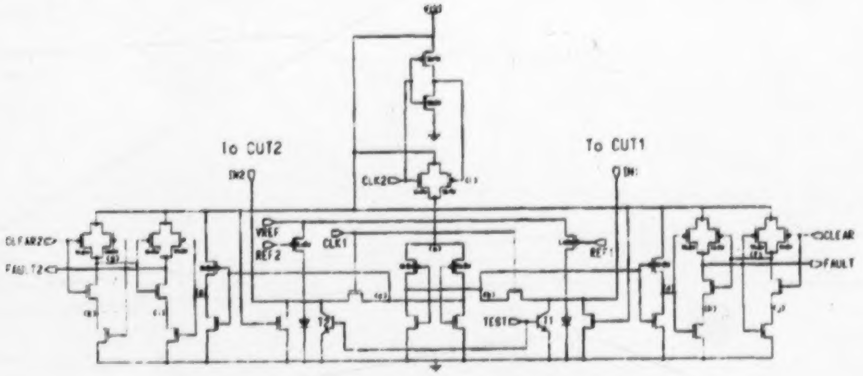

Figure 4.7: BICS proposed by Hurst and Singh [63]

Then, the output is cleared by pulsing the *CLEAR* line low. The *CLEAR* input only works on the side with the low latch result, as occurs when indicating 'no-fault'. For the other side the *FAULT* line remains latched high regardless. For large switching currents, the voltages at the BICS input nodes start out at about the same level of 0.7 V, due to the nonlinear I-V characteristic of the diodes. As the transient currents dissipate, the voltages settle toward zero. Any constant current that is flowing on either side becomes apparent because the voltage on that side decays instead going toward some finite value. A differential measurement may be taken at any time during this decay, depending on the sensitivity of the measuring circuit. The authors claim 31 MHz testing speed and good performance in a variety of environments, as long as the circuit under test (CUT) partitions are reasonably matched with respect to size and capacitance.

J. Kim *et al.* [87], [86] presented a BICS shown in Figure 4.8 based on the current mirror circuit. The proposed BICS first compares a quiescent state current consumed by the CUT with a reference current, I_{REF}. The circuit consists of three NMOS transistors, two PMOS transistors, a constant reference current source, and one inverter. The NMOS transistor, Q_0, is operated as a switch, either isolating or connecting the BICS to the circuit under test. When transient peak appears at the input of the BICS, NMOS current mirror pairs, Q_1 and Q_2, have a minor effect on dynamic current, since the switch transistor, Q_0, is turned on. The NMOS current

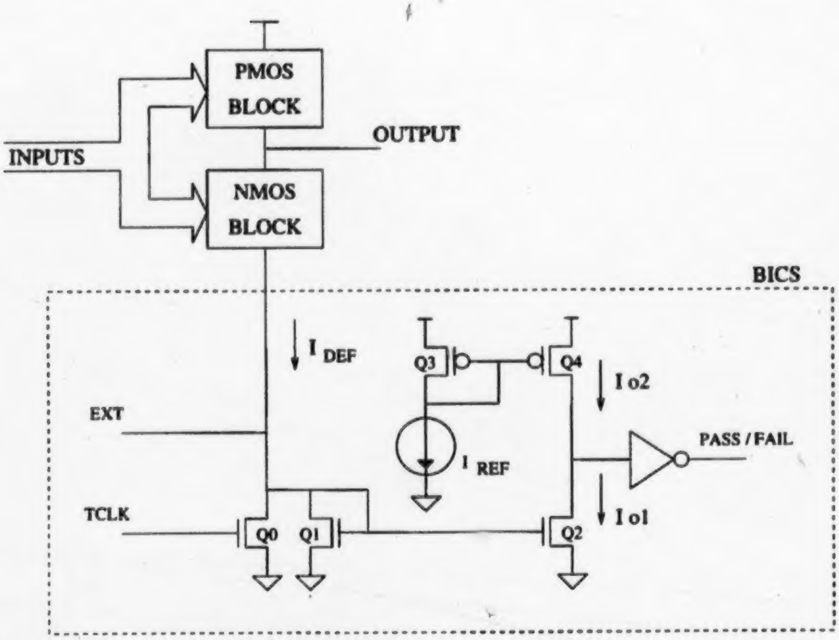

Figure 4.8: BICS proposed by J. Kim *et al.* [87]

mirror pairs, Q_1 and Q_2, replicate the defective current, I_{DEF}. The PMOS current mirror pairs, Q_2 and Q_3, replicate constant reference current I_{REF}. The drains of the PMOS replicating transistor and the NMOS replicating transistor are connected to the input of the inverter to generate the $PASS/FAIL$ signal. The constant reference current is the same as the quiescent state current when the CUT is defect-free. When the quiescent state current, I_{DEF}, is greater than the reference current, I_{REF}, the output signal $PASS/FAIL$ is set to '1', which indicates the existence of defects. The BICS requires three extra pins EXT, $TCLK$, and $PASS/FAIL$. Since the BICS is inserted in series with the CUT, it causes a voltage drop and a large capacitance between the CUT and the substrate. These effects cause the performance degradation and ground level shift. To reduce these undesirable effects, the proposed BICS adds an extra pin EXT to the circuit. EXT is grounded in the normal mode and is floating in the testing mode. The design implemented in 5 V CMOS 0.8 μm n-well process demonstrated operating speed of 25 MHz.

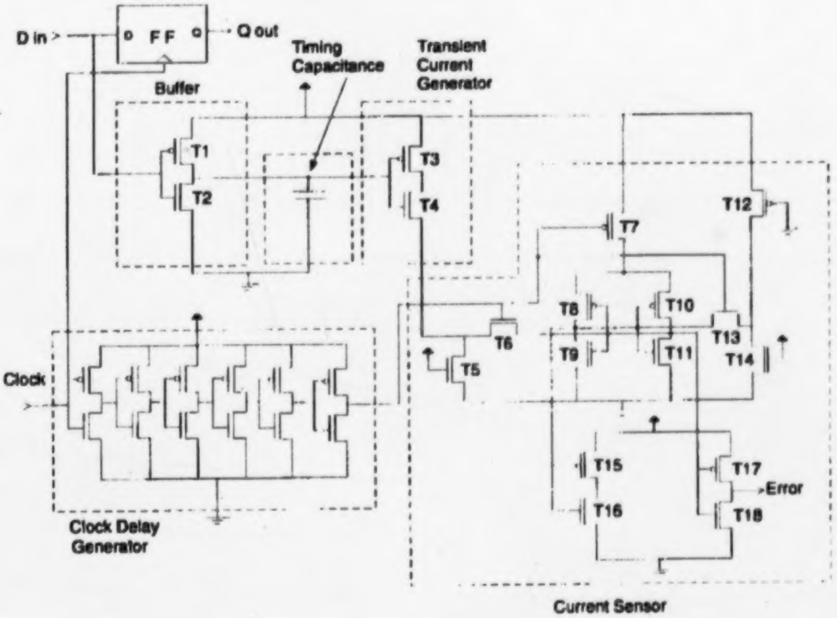
D in
D FF Q
Q out
Timing Capacitance
Transient Current Generator
Buffer
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
Error
Clock
Clock Delay Generator
Current Sensor

Figure 4.9: BICS proposed by Knight and Singh [89]

H. Kim *et al.* [85] have presented a built-in current sensor based on a magnetic FET used to indirectly measure the current. This non-invasive approach is not supposed to produce any CUT performance degradation. However, the authors report difficulty in implementation and sensor's sensitivity to leakage current, which causes large drifts in the calibration circuit.

Knight and Singh [89] implemented a 5 V 2 μm CMOS-based error detection circuit, Figure 4.9, which detects and signals flip-flop's setup or hold timing violation. Changes in input signal D_{in} generate transients which are evaluated by the current sensor with respect to a clock edge. The current from the buffer passes through T_5 whose gate is connected to power supply line. This transistor serves as a resistor that converts the current to a voltage. The sensor measures this voltage and compares it to the reference voltage. The reference voltage is created by proper sizing of transistors T_{14} and T_{12}, which are connected between power and ground and turned on to create a constant current. The sensor consists of two inverters connected in a latch configuration connected to power through T_7, which serves as a switch. The measured voltages are connected to the sensor through pass transistors T_6 and T_{13}. When the delayed clock signal is high, the T_6 and T_{13} are turned on and T_7 is turned off. This allows the charge from the measured voltages to build up on the inverter inputs, but the output is not affected because when T_7 is off, there is no power. When the clock falls, T_6 and T_{13} turn off, which latches the voltages into the inverter inputs. The power to the inverters is also turned on at this time because T_7 is turned on when the clock falls. When the inverters are powered up, the inverter with the higher input voltage dominates, and its output is pulled low. The outputs from both inverters are connected to another set of inverters (T_{15}-T_{18}), which serve to buffer the sensor output from the rest of the circuit. If the current from the current generator is greater than the reference current, then the output of T_{10} and T_{11} is pulled high, and active-low *Error* signal goes to zero which indicates a potential error.

Lechuga *et al.* [93] proposed an I_{DDT} BICS for mixed-signal circuits based on the current mirror which is able to process the highest frequency components in the dynamic power supply current of the circuit under test (CUT). The BICS adds to the resistive sensor an inductance made from a gyrator and a capacitor to carry out the current to voltage conversion. The authors reports an improved fault coverage in continuous circuits and switched current circuits.

Two simple built-in current sensors operating at 3 V and 5 V implemented in a 0.8 μm CMOS process for I_{DDQ} testing are proposed by Lee *et al.* in [95] and [96]. Compared with other methods, authors claim that these designs have lower sensitivity to parameter deviation caused by process or temperature variations. In addition, they provide scalable sensing resolutions and programmable current reference. Experimental results show that a test response time of less than 2ns can be acquired when the faulty I_{DDQ} current is higher than 250 μA.

Lo and Nicolaidis *et al.* [103], [132] proposed an application-specific CMOS built-in current sensor based on self-exercising concept. The BICS performs concurrent monitoring of static current and detects the leakage current which accom-

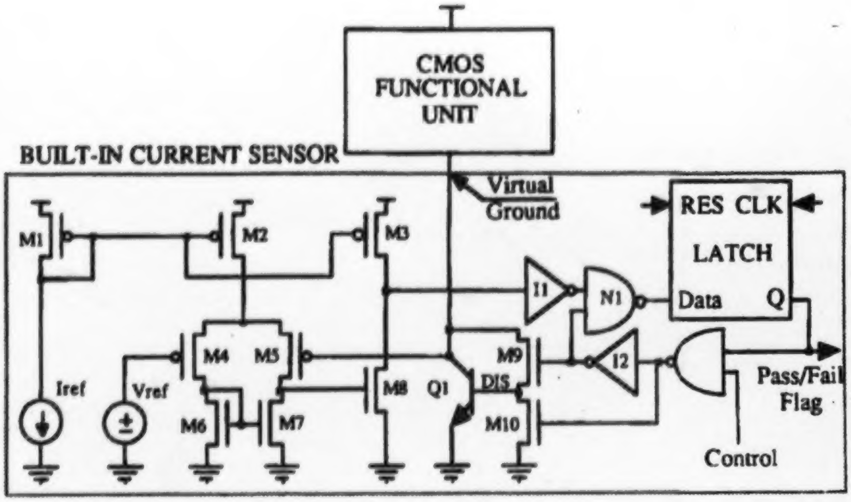
CMOS FUNCTIONAL UNIT
BUILT-IN CURRENT SENSOR
Virtual Ground
RES CLK
LATCH
Data Q
M1
M2
M3
I1
N1
M4 M5
M9
I2
Iref
Vref
M8 Q1
DIS
Pass/Fail Flag
M6
M7
M10
Control

Figure 4.10: BICS proposed by Maly and Patyra [110]

panies the parametric shifts. The authors identified a most challenging problem as the elimination of the extra delay due to the inclusion of BICS.

A compact built-in current sensor based on a slightly modified latch comparator is proposed by Lupon *et al.* in [105]. The design implemented in the 5 V 1.5 μm CMOS process allows detection of excessively high quiescent current without the need for a voltage reference. The sensor requires a silicon area of about $160x9O\ \mu m^2$. The sensing is utilized by a NMOS devices connected between the ground and the CUT. The authors report CUT ground distortion on switching transients of 625 mV for currents up to 3 mA. Lower distortion may be achieved by increasing the width of the NMOS transistor used as a drop element.

A CMOS built-in current sensor proposed by Maidon *et al.* in [107], [106] targets low power supply current monitoring and low power supply voltage mixed circuits. It takes advantage of the parasitic resistor attached to an interconnection layer. The sensor was fabricated in 0.6 μm technology.

The BICS proposed by Maly and Patyra in [110] is shown in Figure 4.10. The design is composed of a voltage drop device (transistor Q_1), comparator (M_1–M_7), a two-stage amplifier (M_3, M_8, I_1), bistable edge-sensitive latch generating flag signal

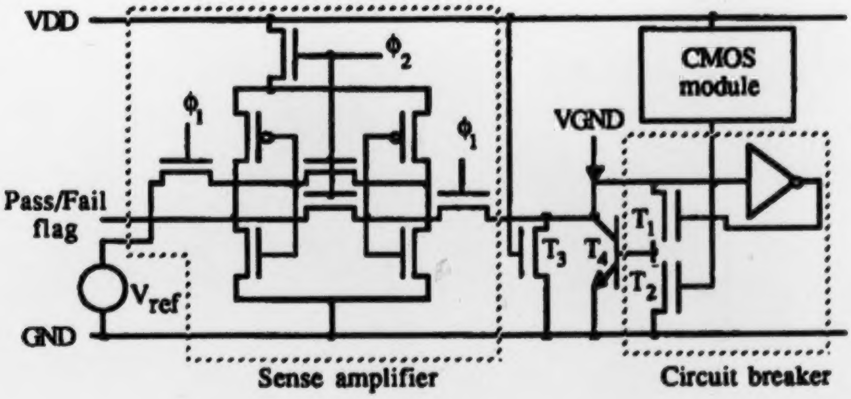

Figure 4.11: BICS proposed by Nigh and Maly [133]

$(PASS/FAIL)$, circuit breaker[3] (M_9, M_{10}, I_2), reference voltage source (V_{REF}), and current source, I_{REF}. One can see that this circuit sets the $PASS/FAIL$ flag at logic '1' and disconnects the CMOS functional unit from ground when V_{ce} of Q_1 is higher than V_{REF}.

The main idea of Maly's design from Figure 4.10 is quite similar to the one proposed by Nigh and Maly in [133] which is shown in Figure 4.11. During normal operation, the NPN transistor T_4 acts as a forward-biased diode, and appears only during transient current peaks as an extra V_{be} drop between the modules virtual ground, V_{GND}, and true ground, GND. When a V_{DD} to GND short is present, the bistable circuit breaker will automatically power-up into its non-conducting state. As the voltage on the V_{GND} node is pulled up, T_2 will turn on, thus beginning to turn T_4 off. As the V_{GND} voltage continues to rise, T_1 eventually switches off as well. The final result of this positive-feedback process is that T_4 will be completely cut off, thus isolating the faulty module from the power supply. The pull-down transistor, T_3, is necessary to ensure that the bistable protection circuitry will power-up into the correct, conducting state. During normal operation, this transistor will not affect

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[3] *A circuit breaker* is a piece of equipment which is designed to protect an electrical apparatus from damage caused by overload or short circuit. Unlike a fuse which operates once and then has to be replaced, a circuit breaker can be reset (either manually or automatically) to resume normal operation.

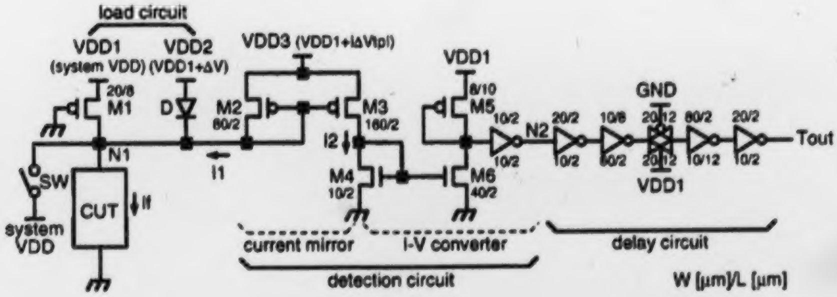

load circuit
VDD1
(system VDD)
VDD2
(VDD1+ΔV)
VDD3 (VDD1+|ΔVtp|)
VDD1
20/8
M1
D
M2
80/2
M3
160/2
8/10
M5
10/2
N2
20/2
10/8
GND
20/12
80/2
20/2
Tout
N1
I1
I2
M4
10/2
M6
40/2
10/2
10/2
80/2
20/12
10/12
10/2
VDD1
SW
CUT
If
system
VDD
current mirror
I-V converter
delay circuit
detection circuit
W [µm]/L [µm]

Figure 4.12: BICS proposed by Miura and Yamazaki [125]

the currents in the circuit significantly. If the BICS is in its non-conducting state, however, this transistor will conduct a small, constant current. The voltage V_{GND} is proportional to the current through the CMOS module, and is compared by a sense amplifier with a reference voltage. The *Pass/Fail* flag is low when the current is normal indicating a fault-free state, and high when the current is abnormally high. The clocks ϕ_1, ϕ_2, and the voltage reference V_{ref} were generated off-chip.

Miura *et al.* presented several 3.3–5 V built-in current sensor designs in [122], [123], [124], [125]. In [123], the authors report sensor's capability to detect 24 μA abnormal I_{DDQ} at $V_{DD} = 5$ V, and 16 μA at $V_{DD} = 3.3$ V. One of their most recent designs published in Journal of Electronic Testing [125], is shown in Figure 4.12. The BICS is composed of three circuits: a small-load circuit, detection circuit, and delay circuit. The small-load circuit consists of a diode and a p-type MOSFET driven by two different power supplies, V_{DD2} and V_{DD3}. This circuit stabilizes the voltage at node N_1, and plays the role of a small load which senses variations of CUT's supply current. The detection circuit detects the abnormal I_{DD} and produces a certain logical value. The delay circuit prevents incorrect output due to a transient current when the gates in the CUT are switching. The voltage at node N_1 is pulled up by using the diode, preventing an excessive voltage drop at N_1. V_{DD2} is set to $V_{DD1} + 0.6\ V$. The p-type MOSFET (M_1), which is driven by V_{DD1}, ensures uninterrupted power supply. The detection circuit consists of a current mirror and an I-V converter driven by different power supplies, V_{DD3} and V_{DD1}. Current I_1

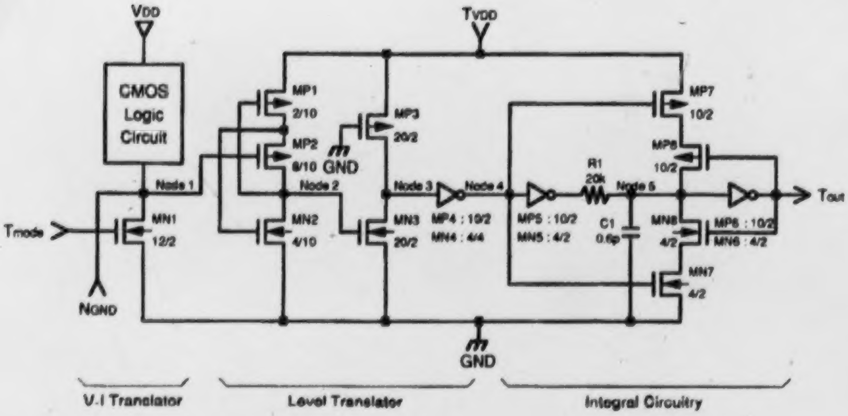

VDD
TVDD
CMOS Logic Circuit
MP1 2/10
MP2 8/10
MP3 20/2
GND
Node 1
Node 2
Node 3
Node 4
Node 5
MN1 12/2
MN2 4/10
MN3 20/2
MP4 : 10/2
MN4 : 4/4
MP5 : 10/2
MN5 : 4/2
R1 20k
C1 0.6p
MP7 10/2
MP8 10/2
MN8 4/2
MP6 : 10/2
MN6 : 4/2
MN7 4/2
Tmode
NGND
Tout
GND
V-I Translator
Level Translator
Integral Circuitry

Figure 4.13: BICS proposed by Miura and Kinoshita [124]

passing through the transistor M_2 is copied by the current mirror; as a result, I_2 flows into M_3. To activate M_2, V_{gs} of M_2 must be higher than its threshold voltage, V_{tp}. Therefore, V_{DD3} is set to a higher voltage than V_{DD1} by, approximately, threshold voltage, V_{tp}. The I-V converter converts I_2 passing through M_3 into a logical value. To prevent generating incorrect output due to the transients, a delay circuit is used instead of a latch circuit seen in other designs. The output of the BICS is delayed by the propagation delay in the delay circuit which produces a high-level output when a high-level input continues for more than a predetermined time interval.

In [124], Miura and Kinoshita proposed another circuit for built-in current testing shown in Figure 4.13. The testing circuit is composed of *V-I translator*, *level translator*, and *integral circuitry*. The V-I translator transforms the CUT supply current to the appropriate voltage signal. The level translator adjust the level of this signal so that it can be processed by the next stage. The integral circuitry flags a fault when a high level of CUT supply current is present longer than a time period specified by the time constant of the integrator, which contains capacitor C_1 and resistor R_1. During the normal mode of operation, $T_{mode} = GND$, $N_{GND} = GND$, and $T_{VDD} = GND$. In test mode, $T_{mode} = V_{DD}$, N_{GND} is floating, and $T_{VDD} = V_{DD}$. The output of the testing circuit, T_{out}, is logic one when the CUT is fault-free, and logic zero when the CUT is faulty. The N_{GND} terminal is open when the CUT is in the test mode, and is connected to system *GND* when the CUT is in the normal mode to reduce the performance degradation. The voltage on *Node* 2 changes as centering on $V_{tn} = 0.6V$ depending on the voltage on *Node* 1. A faulty current threshold is determined by the sizes of MP_1, MP_2, and MN_2. The sizes of inverters are determined so that their threshold voltages are $V_{DD}/2$. *Node* 5 charges and discharges during the time determined by the time constant, τ. If the high logic level on *Node* 4 continues for more than the time interval determined by τ, then *Node* 5 falls below $V_{DD}/2$, and, as a result, T_{out} changes to the logic zero.

Pecuh *et al.* [138] proposed an on-chip low-power circuit for both quiescent and transient current monitoring. The authors report a small area overhead. The monitor is designed for low-voltage digital CMOS circuits (1.5V). The same design can be used in the testing of analogue and mixed signal circuits. Testing speeds of up to 25 MHz can be achieved (including the 4-bit A/D converter, 100 MHz without the converter). The monitor has been implemented in 0.5 μm and 0.35 μm CMOS technology and tested on parallel chains of inverters as circuit under test.

In [141], Picos *et al.* presented experimental results on a built-in current sensor for dynamic current testing, based on integration (charge) concepts. The experimental validation proposed in this work is done through a VLSI CMOS circuit implemented in a 0.7 μm technology. The authors recognize that further design improvements are required to obtain high speed transient sensors.

Two types of built-in current sensors are analyzed by Rius and Figueras in [157]: one based on a simple p-n junction as a sensing element (DBICS) and the other based on a lateral bipolar junction transistor (PBICS). Estimated values are compared with experimental results in circuits built in 1.5 μm technology. The experimental results show a good dynamic PBICS behavior up to 8 MHz with sensitivity of 4.49 mV/μA. When the DBIC sensor is used, the maximum frequency allowed is dependent on the R value and a maximum frequency of 10.5 MHz was obtained with 1.187 mV/μA sensitivity and 2.8 MHz with 4.826 mV/μA sensitivity.

Two current sensor circuits have been presented by Rubio *et al.* in [161] for the application of quiescent current inspection techniques to VLSI testing. The first is

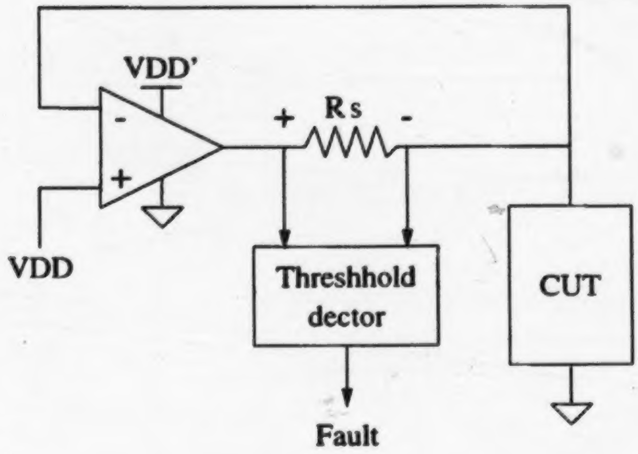


Figure 4.14: BICS proposed by Tang *et al.* [195]

a non-built-in circuit that can be used in environments with classical ATE and any class of digital CMOS integrated circuit. The circuit gives through an input node of the ATE equipment information about the quiescent current test for every test pattern. The second circuit is oriented to BIST circuits (BISC).

A built-in 5 V 1.5 μm CMOS dynamic current sensor for digital integrated CMOS circuits has been proposed by Segura *et al.* in [172]. Sensor behavior is supposed to be independent of DUT parasitics so it can be used with large integrated circuits. The author reports testing frequency of 1 MHz.

An on-chip dynamic power supply current sensor for balanced current-mode analogue circuits has been presented by Sidiropulos *et al.* in [184]. Based on simulation results, the authors conclude that the new approach provides fault coverage comparable to that achieved by previous methods based on a similar principle, but with a much cheaper solution since no additional external equipment is required.

Siskos and Hatzopoulos in [186] presented a very simple 2.5 V BiCMOS current sensor for on-chip current monitoring giving a precise analog output proportional to the quiescent current. Simulations show feasibility of the sensor to operate at high frequencies. Due to its simplicity, the sensor's silicon area overhead is very small.

Table 4.1: Comparison of Several Proposed Current Sensors [195]

Characteristics	Favalli's	Maly's		Miura's	Shen's	Verhelst's	OPA-BICS
	[9]	[8]	[11]	[12]	[13]	[14, 24]	
Primitives used	(2×#gates +1) Trs.	13 Trs. +1 Inv.	10 Trs.+2 Inv. + 2 NAND	16 Trs. 1 R. + 1 C	13 Trs. + 1 D	17 Trs.	24 Trs. + 1 R
Area(μm^2)	8×10^3 *	NA	NA	134×89	8294	NA	328×246
Process	λ	3μm	3μm	2μm	2μm	0.7μm	0.8μm
Clock	×	✓(2)	✓(2)	×	✓(2)	×	✓(1)
Mode select	✓	×	✓	✓	×	×	×
CUT degradation	NA	≤25%	NA	NA	≤14.4%	NA⊕	negligible
Technology	FCMOS	BiCMOS‡	BiCMOS‡	FCMOS	FCMOS	FCMOS	Any
Sampling Rate	NA	20MHz	NA	30MHz	30MHz§	80KHz	>50MHz
Testability	×	×	×	Δ	×	×	Δ
Resistor	×	×	×	✓	×	×	✓
Capacitor	×	×	×	✓	×	×	×
V/I ref.	×	✓	✓	×	✓	✓	×
Resolution	NA	50μA	NA	50μA	80μA	NA	<140μA (Scalable)
Control Pin	1	3	5	3	3	2	≤3
Output Pin	1	1	1	1	2	1	1
Com. V_{DD}/GND	✓ / ×	✓ / ×	✓ / ×	✓ / ×	✓ / ×	× / ✓	✓ / ✓

Note: *- calculated by 114×157×49.18% as estimated by [10], ⊕: The VDD degradation is about 100mV, ‡-lateral NPN/CMOS

§-2ns detection time, ✓-Need or Yes, ×-Does not need or No, Δ-the test for BICS itself is given

In [195], Tang *et al.* proposed the 0.8 μm *OPA – BICS* CMOS design for built-in current sensor shown in Figure 4.14. Due to the properties of an operational amplifier, the voltage at the non-inverting node is approximately equal to the voltage of the inverting node, and no current flows into or out of V^+ or V^- ($I^+ = I^- = 0$). The V^+ of the amplifier is connected to the original power supply level and the V^- is connected to the V_{DD} node of the CUT. This amplifier is powered by an additional pair of power supplies, V'_{DD} and V_{SS}, where V'_{DD} must be higher than V_{DD}, and V_{SS} is common-grounded with other BICS modules. For example, if the CUT operates at the standard power supply level (3 V/0 V) then V'_{DD}, can be designed to work at a 5 V level. Theoretically, the CUT can be operated at the same performance level as the circuit without the BICS if the operational amplifier is ideal. A series resistor R_S, is connected between the output node of the amplifier and the V_{DD} node. The voltage drop on R_S is proportional to power supply current. This implies that various

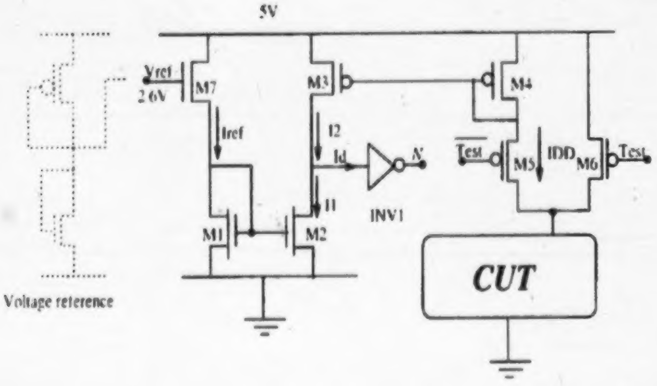


Figure 4.15: BICS proposed by Lee and Tang *et al.* [96]

values of R_S could be selected, depending on the resolution requirement. Authors provided a comparison of various current senors which is shown in Table 4.1.

Lee and Tang in [96] presented a current sensor based on the current-mode design. The sensor circuit is shown in Figure 4.15. The BICS consists of two current mirrors (M_1, M_2) and (M_3, M_4), inverter INV_1, normal/test mode selector, M_5 and M_6, reference current generator transistor M_7, and optional voltage reference circuit. The first current mirror (M_1, M_2) copies the reference current I_{ref} to I_1, while the second mirror (M_3, M_4) is used to mirror the I_{DD} current to I_2. The INV_1 is used as a current comparator. Functionally, $I_d = I_2 - I_1$, and this current will charge or discharge the input of inverter INV_1, depending on the I_d direction. Due to the fact that the input impedance of the inverter INV_1 is almost infinite, the I_d current will be very small and $I_1 \approx I_2$. If $I_{ref} \neq I_{DD}$, only one of the current mirrors will operate, *i.e.*, either I_{ref} or I_{DD}. Assuming initially $I_{ref} = I_{DD}$, then $I_1 = I_2 = I_{DD}$. When I_{ref} increases, the gate voltage on M_1 and M_2 will increase, which results in the increase of the gate-source voltage of M_2: Therefore, I_1 will become greater than I_2 and the input of INV_1 will be immediately discharged, which results in a logic '1' flag at node N. Conversely, if I_{ref} decreases to less than I_{DD}; node N will be pulled-down. Because of the high input impedance of the current comparator and the utilization of current mirror, even a very small difference between I_{ref} and

I_{DD} will be distinguished, which means the BICS can achieve good resolution. The input capacitance of the INV_1 determines the detection speed of the sensor.

Vázquez and Gyvez in [208] implemented a 0.18 μm CMOS built-in current sensor design for ΔI_{DDQ} testing. This implementation has three distinctive features: 1) built-in self-calibration to the process corner in which the circuit under test was fabricated; 2) digital encoding of the quiescent current of the circuit under test; and 3) implementation of two ΔI_{DDQ} testing algorithms.

Many patents describing different topologies and types of current sensor circuits can be found, too. A patent filled by Lee *et al.* [97] describes a built-in current sensor for I_{DDQ} monitoring which includes a reference current generator, two current mirrors, an inverter, and a multiplexer to switch between the normal circuit operation mode and the test mode. Maly *et al.* invented a built-in current sensor which is provided to sense abnormal quiescent current flow through the integrated circuit while ignoring normal high current peaks [111]. A sensor patented by Needham *et al.* [131] utilizes a magnetic sensor circuitry which is not series-coupled to the circuit under test. The magnetic field sensor is located on the substrate near the supply line of the integrated circuit and detects the magnetic field generated from the supply line current. The monitor produces a measurement result calibrated to indicate when I_{DDQ} has a predetermined value. Manhaeve *et al.* in [49] disclosed a system for high-resolution measurements of a supply current of an electronic circuit. The system comprises a bypass unit, a second generation current conveyor based measurement unit, a comparison evaluation unit, and an optional latch unit to hold the measurement result until the result of the next measurement is valid.

The preceding survey of the proposed designs clearly reveals that all of the described circuits require a sensing element, usually a resistor, and a fast amplifier to achieve effective current sensing performance. In the next chapter, we present a novel current amplifying cell based on the application of the current conveyor, and a new built-in current sensor amplifier topology suitable for current monitoring test applications.

Chapter 5

Current Amplifier Design

5.1 Introduction

The fundamental signal-processing function employed in almost every electronic system is signal amplification. Numerous types of amplifiers have been known for a long time and their behavior, design, and properties is a well-researched topic [26]. The demand for low-power, low-voltage analog integrated circuits has increased in all areas of applications [217]. With the latest technologies, the power supply voltage of core digital devices is scaled to the level of 1 V. The reduction in digital supply voltages has inherently carried over to analog systems, where the design limitations have become more severe.

In addition, including the analog and digital circuitry on the same substrate has become a standard practice in the industry as a way to reduce the cost. Through the continuous technology expansion, system-on-chip (SoC) emerges as a structure that provides the level of integration far beyond traditional mixed-signal devices. The high level of integration, decreased supply voltages, and constraints with respect to power consumption impose significant challenges for analog design in general. Some well-known and long-time existing design techniques have become unattainable in the low voltage environment. For example, low supply voltages necessitate the use of cascading rather than cascoding, for achieving high gain at moderate and high frequencies. Apparently, there is a strong need for new low-voltage amplifiers that maintain similar performances with respect to ones with higher voltage

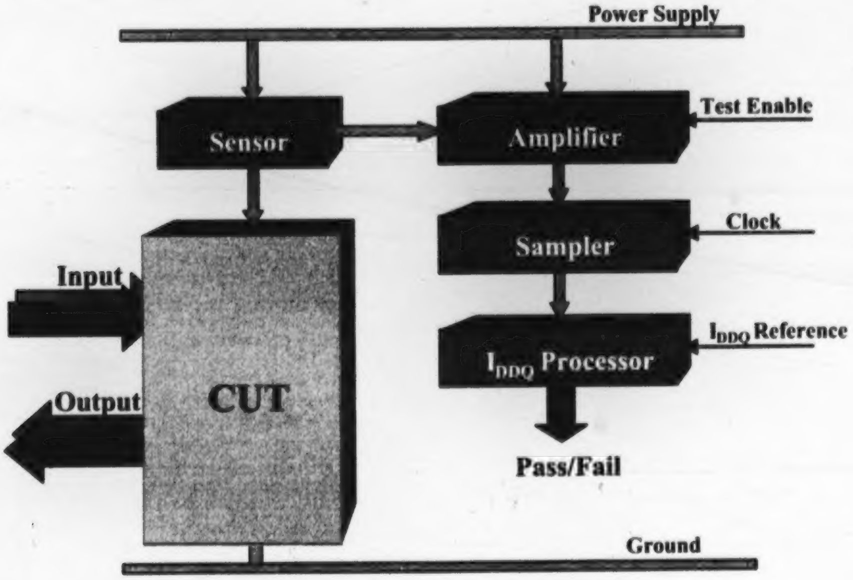

Power Supply
Sensor
Amplifier
Test Enable
Clock
Sampler
I_{DDQ} Reference
I_{DDQ} Processor
Input
Output
CUT
Pass/Fail
Ground

Figure 5.1: Typical monitoring environment

supplies.

As described in Chapter 4, Section 4.2 (page 68), strict requirements for efficient current monitor design pose a significant challenge for a designer. In this chapter, we propose an amplifier topology suitable for power supply current monitoring, the technique well established in many application areas such as testing, quality control, security, *etc.*.

In a typical monitoring environment, shown in Figure 5.1, the circuit under test (CUT) is connected to the power supply through the sensor. The amplifier receives a signal from the element which senses variations of the power supply current I_{DD}. In the presence of a defect, the level and shape of I_{DD} current changes, indicating a defective device.

Presently, a significant limitation to production application of current monitoring is the speed at which measurements can be made [6]. The availability of highly linear devices capable of operation at today's high frequencies, with the sensitivity in a micro-ampere range, presents one of the key issues in the efficient application of the current monitoring technique. Moreover, the ultra low-voltage environment makes the design difficult, which explains the lack of transimpedance or current amplifiers suitable for such applications. Yet another challenge in the monitoring of highly integrated devices and SoC architectures is reduced accessibility and controllability of internal cores. A built-in methodology for IC monitoring is considered presently the most efficient way to overcome existing problems [192].

As described in Section 4.6 on page 77, sufficient research has been devoted to the development of effective current monitor topologies, and many schemes have been proposed. Although the current sensing ability has been enhanced, there are still many unsolved problems. For example, many designs have been proposed for older technologies which assume higher power supplies. Such designs can not be utilized in deep sub-micron battery-operated environments. A noticeable setback may be the impact on the circuit under test and its performance when a sensor is placed in a power supply line. The development of effective built-in current monitors depends on our ability to design an amplifier that meets the requirements outlined in Chapter 4, Section 4.2 (page 68), namely, low area overhead, negligible performance loss, reasonable power dissipation, capability of high-frequency measurements, high sensitivity, and low distortion. In this chapter, we propose a solution that satisfies these requirements. We present a novel built-in amplifier topology that could be successfully employed in a current monitoring scheme as a front-end device of the built-in monitoring system (*i.e.*, sensing and detection device).

5.2 Current Amplifier

The amplifier, shown in Figure 5.2, is based on the novel current amplifying cell (transistors M_1 to M_9) supported by an additional gain stage (M_{N1}, M_{N2}, M_{N3}, M_{P1}, M_{P2}, and M_{P3}) and the source follower input stage (M_{SF} and R_F) [36]. R_F resistor is chosen to set the bias of the next amplifying stage (*Stage II*) with $V_S \approx \frac{1}{2}V_{DD}$ (a current source could be used, also). Table 5.1, Table 5.2, and Table 5.3 list the values of circuit parameters of implemented 0.13 μm and 0.18 μm designs for *Stage I*, *Stage II*, and *Stage III*, respectively.

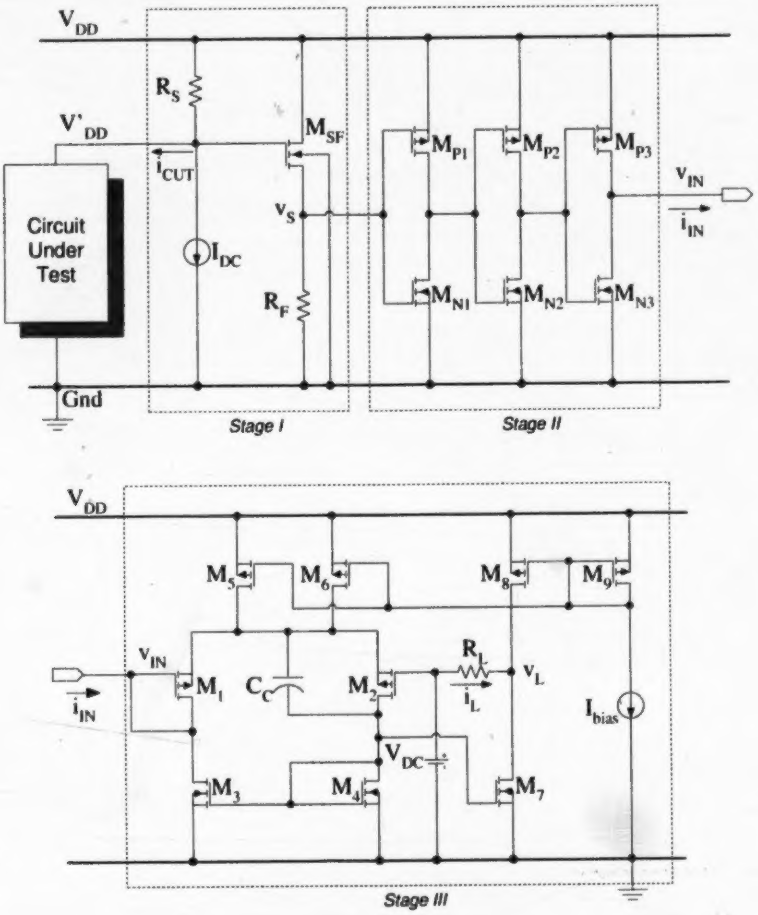

V_DD
V'_DD
R_S
M_SF
i_CUT
v_S
I_DC
R_F
Circuit Under Test
Gnd
Stage I
M_P1
M_P2
M_P3
M_N1
M_N2
M_N3
v_IN
i_IN
Stage II
V_DD
M_5
M_6
M_8
M_9
v_IN
i_IN
M_1
C_C
M_2
R_L
v_L
i_L
I_bias
V_DC
M_3
M_4
M_7
Stage III

Figure 5.2: Current monitor amplifier schematic

The resistor $R_S = 50\ \Omega$ is chosen as a current sensing element. The sensing element (as well as the current amplifier) is susceptible to temperature and process variations. This could negatively affect the result of the monitoring process where accurate measurements are required. Several techniques have been proposed to minimize the impact on accuracy of measurements and improve the decision process. A differential current monitoring approach significantly reduces potential implications of temperature or process variations by processing the difference of

Table 5.1: Specification of Design Parameters – *Stage I*

Source Follower		**0.18 μm Design**	**0.13 μm Design**
M_{SF} (W/L)	[μm/μm]	8/0.18	9/0.13
R_F	[Ω]	2k	1.5k
R_S	[Ω]	50	50

Table 5.2: Specification of Design Parameters – *Stage II*

Second Gain Stage		**0.18 μm Design**		**0.13 μm Design**	
M_{P1} (W/L)	[μm/μm]	2/0.18	$m = 10$	2/0.19	$m = 16$
M_{P2} (W/L)	[μm/μm]	1.6/0.18	$m = 10$	1.6/0.13	$m = 12$
M_{P3} (W/L)	[μm/μm]	3.2/0.18	$m = 10$	3.2/0.13	$m = 19$
M_{N1} (W/L)	[μm/μm]	0.5/0.18	$m = 10$	0.5/0.19	$m = 16$
M_{N2} (W/L)	[μm/μm]	0.5/0.18	$m = 10$	0.5/0.13	$m = 12$
M_{N3} (W/L)	[μm/μm]	0.5/0.18	$m = 10$	0.5/0.13	$m = 19$

two current measurements [144]. In this case, if the resistance of the sensing element increases due to the temperature, all current measurements will be elevated, but their differences should remain the same for defect-free circuits. Another simple, yet efficient measure to counter the effect of temperature variations is to layout R_S as a series connection of two resistors with opposite temperature coefficients (*e.g.*, resistive poly with positive and N-diffusion with negative temperature coefficient) [39].

Current I_{DC} represents the offset current which sets the operating point of *Stage I*. Current i_{CUT} denotes the total power supply current of the monitored system. When the power supply current is drawn by the system, it produces a voltage drop across the resistor. This voltage drop is transferred through the NMOS source follower to the next amplifying stage (*Stage II*). The follower provides a wide-band gain frequency characteristic. However, as a disadvantage, the transistor M_{SF} contributes quite considerably to the total noise which, in turn, lowers amplifier's dynamic range especially at lower frequencies.

Since the substrate of M_{SF} is not tied to the source, the body effect occurs. Tak-

Table 5.3: Specification of Design Parameters – *Stage III*

Current Amplifying Cell		**0.18 μm Design**	**0.13 μm Design**
M_1 (W/L)	[μm/μm]	80/0.5 $m = 1$	80/0.13 $m = 1$
M_2 (W/L)	[μm/μm]	8/0.5 $m = 1$	8/0.13 $m = 1$
M_3 (W/L)	[μm/μm]	20/0.5 $m = 1$	20/0.13 $m = 1$
M_4 (W/L)	[μm/μm]	2/0.5 $m = 1$	2/0.13 $m = 1$
M_5 (W/L)	[μm/μm]	80/0.5 $m = 1$	80/0.13 $m = 1$
M_6 (W/L)	[μm/μm]	8/0.5 $m = 1$	8/0.13 $m = 1$
M_7 (W/L)	[μm/μm]	86/0.5 $m = 1$	81/0.13 $m = 1$
M_8 (W/L)	[μm/μm]	300/0.5 $m = 1$	300/0.13 $m = 1$
M_9 (W/L)	[μm/μm]	8/0.5 $m = 1$	8/0.13 $m = 1$
R_L	[Ω]	1	1
V_{DC}	[V]	0.9	0.6
I_{bias}	[μA]	10	35

ing into account the body transconductance $g_{mb_{SF}}$ of M_{SF}, a low-frequency small signal gain of the source follower can be expressed as

$$\frac{v_s}{i_{ms}} = \frac{g_{m_{SF}}(R_F \parallel r_{o_{SF}})R_S}{1 + (g_{m_{SF}} + g_{mb_{SF}})(R_F \parallel r_{o_{SF}})} \tag{5.1}$$

where v_s denotes the source voltage, $g_{m_{SF}}$ is the transconductance, and $r_{o_{SF}}$ represents the incremental output resistance of M_{SF}. The second stage low-frequency voltage-to-current ac gain is

$$\frac{i_{in}}{v_s} = -g_{m_1} r_{o_{NP_1}} r_{o_{NP_2}} r_{o_{NP_3}} g_{m_{NP_1}} g_{m_{NP_2}} g_{m_{NP_3}} \tag{5.2}$$

where output resistance $r_{o_{NP_x}} = r_{o_{N_x}} \parallel r_{o_{P_x}}$ and transconductance $g_{m_{NP_x}} = g_{m_{N_x}} + g_{m_{P_x}}$, for $x = 1, 2, 3$. The current i_{in} denotes the AC component of the second stage output current i_{IN}, which is, also, the input current of the third stage.

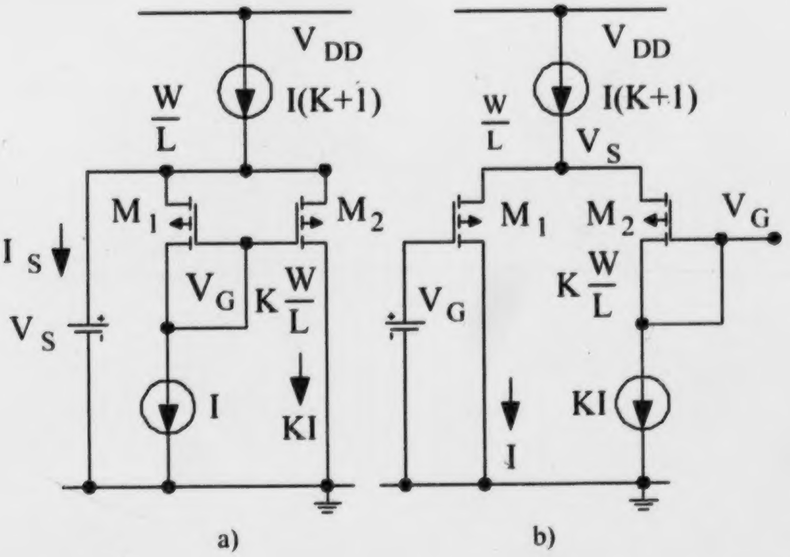
5.3 Current Amplifying Cell

The new current amplifying cell (*Stage III* in Figure 5.2) is designed as the core circuitry of the amplifier. It is based on application of the current conveyor [26],

[200], [92], [194]. The gain of the cell should be well defined in the bandwidth that starts from zero and goes to very high frequencies. Also, the cell should be easily (preferably, directly) cascaded with other similar cells (this is why we call it 'amplifying cell'). To arrive at our goal, we decided to use a CMOS current conveyor in the inverse mode of operation. The input signal is a current, and it is supplied to the terminal that was used for connection of the voltage-to-current converting resistor. The terminal that was previously used for application of the input voltage signal is now connected to the reference or ground potential. The terminal with output current is used as in ordinary applications of a current conveyor. These modifications resulted in a new wide-band CMOS current amplifying cell satisfying the above formulated requirements.

The cell has a current gain that depends on transistor dimensions only. To increase the gain the cells can be cascaded directly. This direct cascading is achieved by using an input stage sub-circuit that can be called a 'voltage mirror'. In a familiar current mirror, shown in Figure 5.3a, the transistor M_2 sources the current KI into the ground line when its aspect ratio is K times larger than the aspect ratio of M_1. If the source potential V_S is specified, then the gate potential V_G can be calculated. This circuit can be inverted, Figure 5.3b, when the current ratio is set. Then, if the gate potential V_G of the left transistor is specified, then the gate potential of the right transistor becomes equal to V_G as well.

This property allows transmission of the voltage from one side of the circuit to another, and, eventually, provides direct cascading of the cells. The cell, in addition to this voltage mirror input stage, includes a common source amplifying stage that amplifies the current developed inside the cell's input stage. The implemented cell is analyzed, and the transfer function for current, cell's input impedance, and transimpedance (for the resistive load) are found. Then, the frequency compensation for optimized frequency response is proposed. The above mentioned frequency dependencies of the cell parameters are calculated for the compensated circuit as well.



a) b)

Figure 5.3: Voltage mirror concept: a) current mirror with specified source voltage b) inverted voltage mirror

5.4 Cell DC and AC Small-Signal Parameters

5.4.1 DC Gain

The cell shown in Figure 5.2 (*Stage III*) includes the input stage (transistors M_1 to M_4) configured as a voltage mirror. This stage is biased by two transistors M_5 and M_6. In practice, these two transistors can be combined into one unit, yet they are shown separately because this representation helps to understand the circuit design. For proper functioning of the circuit, it is required that the following aspect ratio requirement be satisfied:

$$\frac{(W/L)_1}{(W/L)_2} = \frac{(W/L)_3}{(W/L)_4} = \frac{(W/L)_5}{(W/L)_6} = M. \tag{5.3}$$

The cell output stage is the common source transistor M_7 loaded by the current source transistor M_8. It is also required that in this stage the following aspect ratio

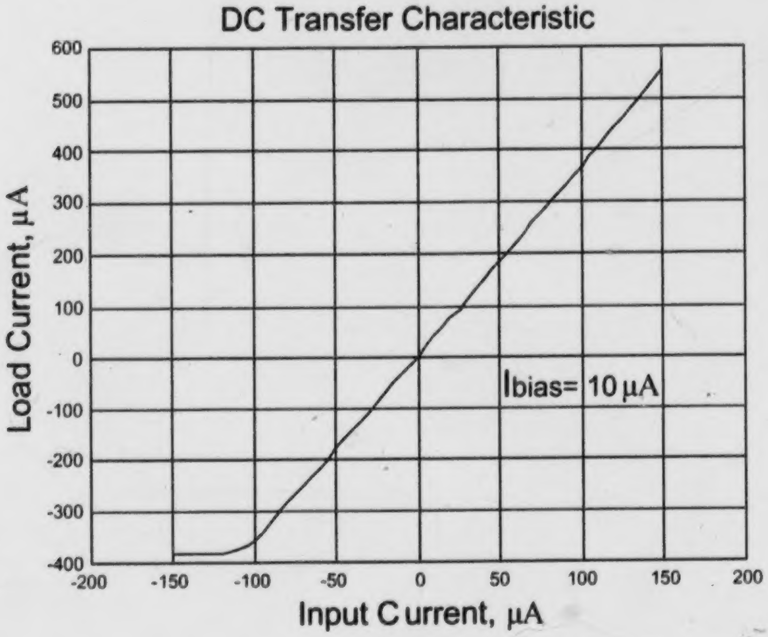


Figure 5.4: Current amplifying cell DC transfer characteristic

relationship be satisfied:

$$\frac{(W/L)_8}{(W/L)_6} = \frac{(W/L)_7}{(W/L)_4} = N. \tag{5.4}$$

If the gate of M_2 is connected to the voltage V_{DC}, then the requirement in Eq. (5.3) provides $V_{IN} = V_{DC}$ at the gate of M_1 when the source of input signal is disconnected. From the other side, if the transistors are ideal, then the condition in Eq. (5.4) results in $I_L = 0$, and $V_L = V_{DC}$ in this case. Hence, the cells of this type can be cascaded directly. In practice, due to transistor asymmetry, one has to slightly tune the sizes of M_7 or M_8, or to introduce an output offset cancelation current source.

Let us calculate the DC gain of the cell. When the input current increases by ΔI, then the current in M_1 decreases, and in M_2 increases by ΔI_1. This ΔI_1 is the difference between the input signal and the feedback signal $M\Delta I_1$. One obtains the

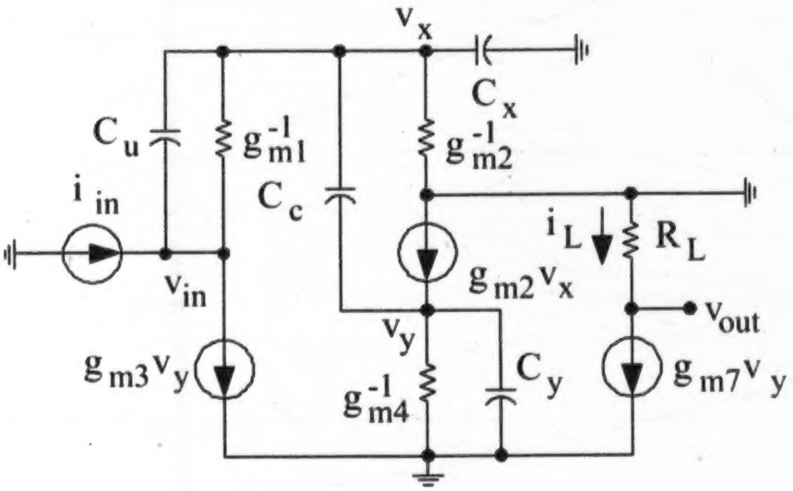


Figure 5.5: Small signal equivalent circuit for compensated cell

equation:

$$\Delta I = \Delta I_1 + M\Delta I_1. \tag{5.5}$$

Hence, one finds that

$$\Delta I_1 = \frac{\Delta I}{M+1}. \tag{5.6}$$

The load current can be found as

$$\Delta I_L = N\Delta I_1 = \frac{N}{M+1}. \tag{5.7}$$

Therefore, the circuit DC gain is equal to

$$K_I = \frac{\Delta I_L}{\Delta I_1} = \frac{N}{M+1}. \tag{5.8}$$

One can see that the cell has a current gain which depends on transistor dimensions only. The circuit transfer characteristic, shown in Figure 5.4, is linear for $\Delta I = \pm 100$ μA with a sharp transition to limit negative input currents. This limit corresponds to the drain current of transistor M_8.

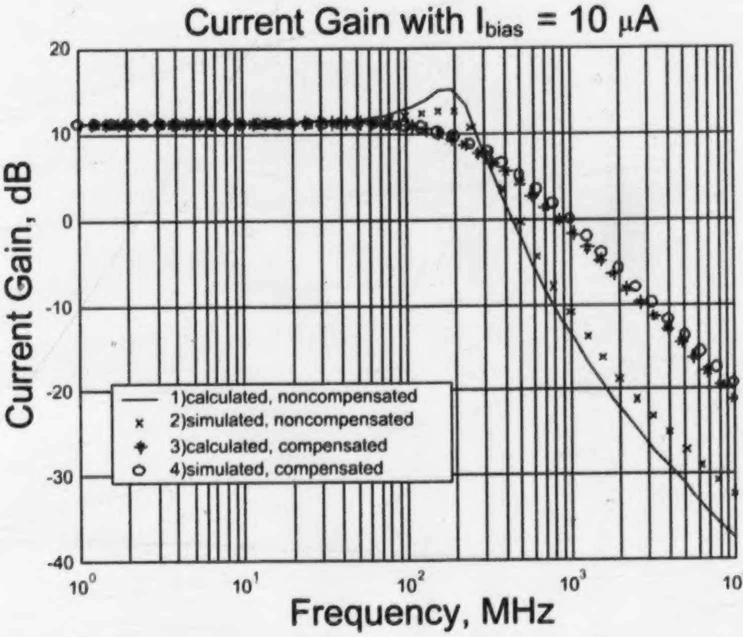


Figure 5.6: Cell's current gain frequency characteristics

5.4.2 AC Low-Frequency Parameters

Let us calculate now a low-frequency small-signal gain and other circuit parameters. The system of equations

$$
\begin{gathered}
g_{m1}v_{in} - g_{m1}v_{sg2} = i_{in} - g_{m3}v_{gs3} \\
g_{m1}v_{in} = (g_{m1} + g_{m2})v_{sg2} \qquad (5.9) \\
g_{m4}v_{gs7} = g_{m2}v_{sg2}
\end{gathered}
$$

describes the input stage, and the equation

$$i_l = g_{m7}v_{gs7} \qquad (5.10)$$

is applied to the output stage of the cell. The system (5.9) can be rewritten as

$$\begin{bmatrix} g_{m1} & -g_{m1} & g_{m3} \\ -g_{m1} & g_{m1}+g_{m2} & 0 \\ 0 & -g_{m2} & g_{m4} \end{bmatrix} \begin{bmatrix} v_{in} \\ v_x \\ v_y \end{bmatrix} = \begin{bmatrix} i_{in} \\ 0 \\ 0 \end{bmatrix} \tag{5.11}$$

where we denoted $v_{sg2} = v_x$ and $v_{gs3} = v_{gs7} = v_y$. From Eq. (5.11) one can find that

$$v_y = \frac{i_{in}}{g_{m3}+g_{m4}}. \tag{5.12}$$

Considering Eq. (5.10) one finds that

$$i_l = i_{in}\frac{g_{m7}}{g_{m3}+g_{m4}}. \tag{5.13}$$

Hence, the low-frequency small-signal ac gain is

$$K_i = \frac{i_l}{i_{in}} = \frac{g_{m7}}{g_{m3}+g_{m4}}. \tag{5.14}$$

The transconductance g_{mi} can be found as

$$g_{mi} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_i I_{Di}}. \tag{5.15}$$

Using Eq. (5.15) for $i = 3,4,7$, the design condition equations (5.3) and (5.4), and considering that $I_{D3} = MI_{D4}$ and $I_{D7} = NI_{D4}$, one obtains

$$K_i = \frac{N}{M+1} = K_I. \tag{5.16}$$

Another important circuit parameter is the low-frequency small-signal input impedance. One can find from Eq. (5.11) that

$$v_{in} = \frac{i_{in}}{g_{m1}}\frac{[1+(g_{m1}/g_{m2})]}{[1+(g_{m3}/g_{m4})]}. \tag{5.17}$$

Using Eq. (5.14) for i=1,2,3,4 and considering that $I_{D1} = MI_{D2}$, and (5.3) and (5.4) are satisfied, one obtains that

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_{m1}}. \tag{5.18}$$

Finally, for the circuit loaded by a load resistance R_L, the circuit transresistance is

$$R_T = \frac{v_{out}}{i_{in}} = K_i R_L. \tag{5.19}$$

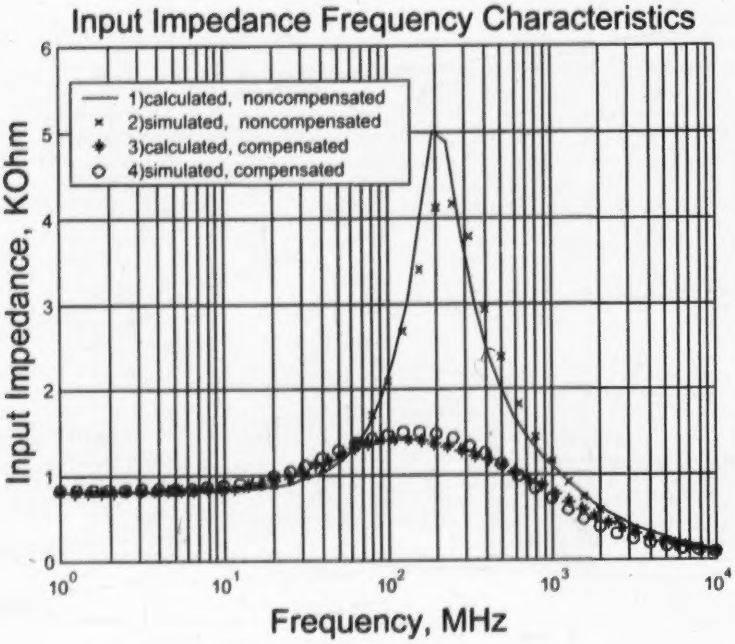


Figure 5.7: Current amplifying cell input impedance

5.4.3 Compensated Frequency Characteristics

The numerical calculations show that the amplitude frequency response of the cell current transfer function has a pronounced peak. This is not always desirable, and to avoid it the circuit should be frequency compensated. This frequency compensation is achieved by placing a compensation capacitor C_c between the source and drain of M_2. When $C_c >> C_{gd3}$, then the M_3 gate-drain capacitor C_{gd3} can be omitted from calculations. The small-signal equivalent circuit for this case is shown in Figure 5.5.

One can find that the current transfer function for this case is:

$$K_i(s) = \frac{g_{m7}}{g_{m3}+g_{m4}} \frac{(1+\frac{s}{\omega_{zc}})}{(1+2\xi_{pc1}\frac{s}{\omega_{pc1}}+\frac{s^2}{\omega_{pc1}^2})} \tag{5.20}$$

where

$$\omega_{zc} = \frac{g_{m2}}{C_c} \tag{5.21}$$

$$\omega_{pc1} = \sqrt{\frac{g_{m2}(g_{m3}+g_{m4})}{C_xC_y + C_c(C_x+C_y)}} \tag{5.22}$$

and

$$\xi_{c1} = \frac{g_{m4}(C_x+C_c) + g_{m3}C_c + g_{m2}C_y}{2\sqrt{g_{m2}(g_{m3}+g_{m4})}\sqrt{C_xC_y + C_c(C_x+C_y)}} \tag{5.23}$$

The lumped capacitors are calculated as follows:

$$\begin{aligned} C_u = {} & C_{gs1} \\ C_x = {} & C_{gs2} + C_{sb1} + C_{sb2} + C_{db5} + C_{db6} + C_{gd5} + C_{gd6} \\ C_y = {} & C_{gs3} + C_{gs4} + C_{gs7} + C_{db2} + C_{db4} + C_{gd2} + \\ & + C_{gd7}(1 + |A_{v2}|) \end{aligned} \tag{5.24}$$

where $A_{v2} = -g_{m7}R_L$ is a second stage voltage gain. The calculated frequency characteristic of the current gain is shown in Figure 5.6.

The input impedance frequency characteristics of the cell is shown in Figure 5.7. It can be expressed as

$$Z_{in}(s) = \frac{1}{g_{m1}} \frac{(1 + 2\rho_{c1}\frac{s}{\omega_{zc1}} + \frac{s^2}{\omega_{zc1}^2})}{(1 + \frac{s}{\omega_{p1}})(1 + 2\xi_{c1}\frac{s}{\omega_{pc1}} + \frac{s^2}{\omega_{pc1}^2})} \tag{5.25}$$

where

$$\omega_{zc1} = \sqrt{\frac{(g_{m1}+g_{m2})g_{m4}}{(C_u+C_x)C_y + (C_u+C_x+C_y)C_c}} \tag{5.26}$$

and

$$\rho_{c1} = \frac{g_{m4}(C_u+C_x) + (g_{m1}+g_{m2})C_y + (g_{m1}+g_{m4})C_c}{2\sqrt{(g_{m1}+g_{m2})g_{m4}}\sqrt{(C_u+C_x)C_y + C_u + C_x + C_y}}. \tag{5.27}$$

The circuit compensation can be also achieved by placing a compensation capacitor across the transistor M_3. This placement corresponds to the compensation approach used in operational amplifiers [73]. In simulations, the results of both methods are practically identical (the value of the capacitor that eliminates peaking is almost the same). Yet, the reader can verify that this placement results in a third-order polynomial for the circuit denominator, *i.e.*, the poles and zeros of the compensated circuit can be calculated only numerically.

The investigation of the proposed cell shows that it has an easy tractable design and good high frequency capabilities. The input impedance can be reduced by increasing parameter M, and the gain can be restored by increasing parameter N in

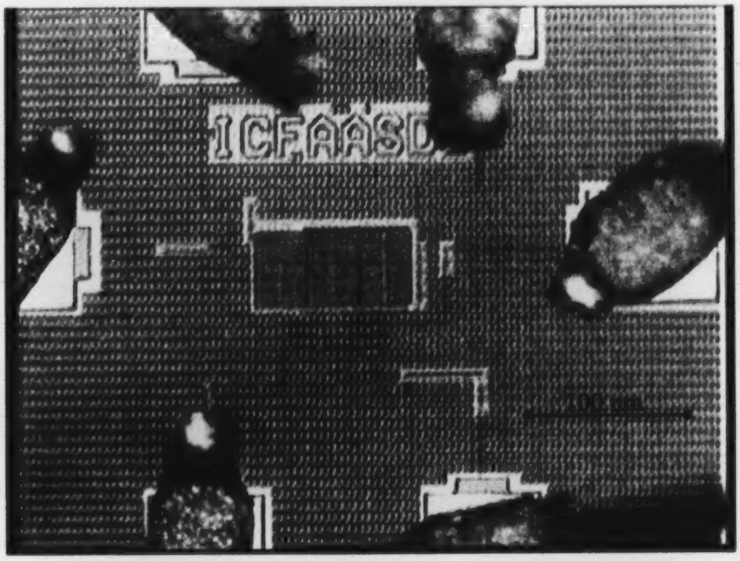


Figure 5.8: Current amplifying cell microphotograph

the design equations (5.3) and (5.4). This reduces the input impedance by $1/g_{m1}$, and the resulting decrease of gain, due to the necessary increase of $1/g_{m3}$, will be compensated by increasing $1/g_{m7}$. The frequency band can be further increased if the bias current (and the power supply current) increases, and the circuit is designed with higher overdrive voltages. In addition, the circuit configuration allows one to add a current divider at the circuit output, and to use the high frequency asymptotic behavior of the current gain for the gain-bandwidth exchange. Finally, the cell was realized in 0.18 μm CMOS technology process (Figure 5.8) to test it separately from the amplifier.

5.5 Amplifier Properties and Scaling

During the course of this research work, five circuit prototypes were fabricated. The microphotographs of some fabricated chips are shown in Figures 5.11-5.14.

The amplifier shown in Figure 5.2 is implemented in two CMOS processes: a 0.13 μm operating at a 1.2 V power supply and 0.18 μm with a 1.8 V power supply

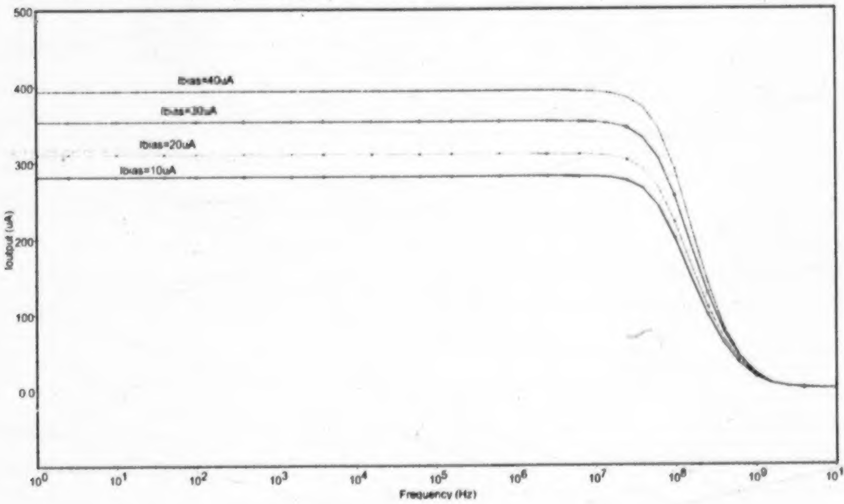


Figure 5.9: 0.18 μm amplifier frequency response for different I_{bias}

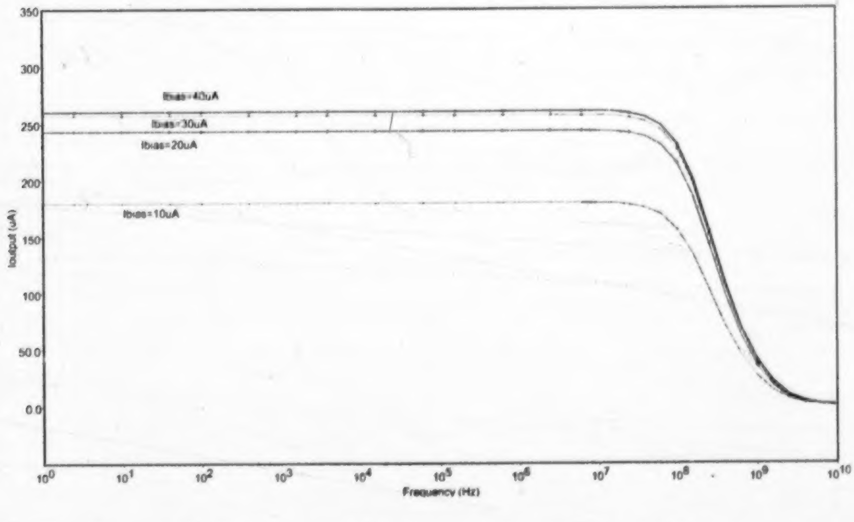


Figure 5.10: 0.13 μm amplifier frequency response for different I_{bias}

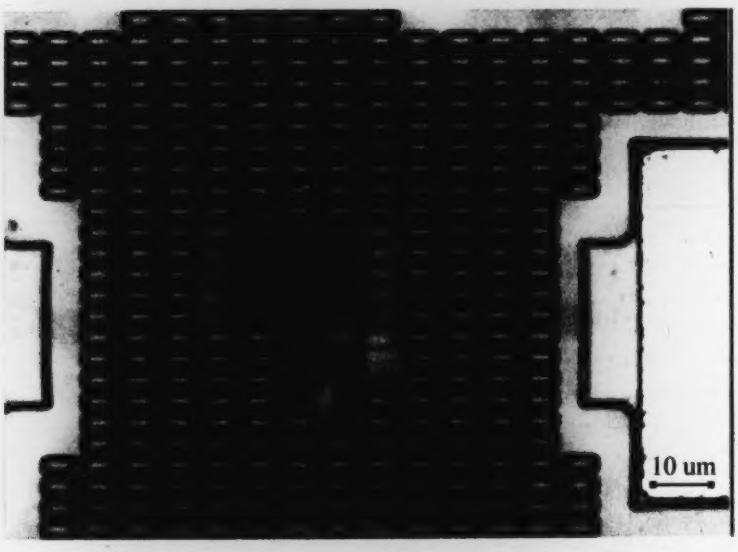


Figure 5.11: Prototype 2 - microphotograph of the sensor's core circuitry

voltage. The first version of the chip was implemented in a 0.13 μm single poly, eight copper metal, salicide logic process (self-aligned silicide process, where both the gate and the source-drain regions are silicided) supporting dual-oxide 1.2/3.0 V operation. The second chip was fabricated in a 0.18 μm dual-oxide, single poly, six metal, salicide CMOS process with a nominal 1.8/3.3 V supply voltage.

We observed the effect of technology scaling on the amplifier's properties with respect to power dissipation, silicon area, DC gain, frequency characteristics, total harmonic distortion, signal-to-noise ratio, dynamic range, and power supply degradation of a monitored system. It was not possible to uniformly scale the amplifier design by using any of the known scaling techniques such as constant field scaling, constant voltage scaling, quasi-constant scaling, or generalized scaling [40]. An attempt to uniformly scale the transistor sizes resulted in an amplifier with significantly degraded properties. Therefore, we decided to optimize the designs with respect to the gain-bandwidth product to power consumption ratio. A detailed comparison of all relevant measured parameters of 0.13 μm and 0.18 μm designs is summarized in Table 5.4.

Table 5.4: Summary of Parameters for the 0.13 *μm* and 0.18 *μm* Designs

General	**0.18μm**	**0.13μm**
Power Supply [V]	1.8	1.2
DC Current [mA]	3.60	4.77
Power Consumption [mW]	6.47	5.73
Die Area [μm x μm]	460x420	450x430
Core [μm x μm]	130x80	130x90
Gain	**0.18μm**	**0.13μm**
DC Gain [dB]	51.89	48.30
Gain at 100MHz [dB]	49.13	47.23
Gain at 500MHz [dB]	35.71	38.89
Gain at 1GHz [dB]	25.58	32.04
Unity Gain Bandwidth [MHz]	3750.00	6780.00
3dB Bandwidth [MHz]	106.20	190.10
Total Harmonic Distortion	**0.18μm**	**0.13μm**
Total Harmonic Distortion at 2μA p-p 100MHz Input [%]	0.82	0.14
Total Harmonic Distortion at 4μA p-p 100MHz Input [%]	1.86	0.3
Main Harmonic RMS at 1μA p 100MHz Input [mA]	2.84E-01	2.30E-01
Worst Harmonic RMS at 1μA p 100MHz Input [mA]	2.29E-03	3.28E-04
Input and Output Swing	**0.18μm**	**0.13μm**
Maximum Input Swing p-p [μA]	12.0	30.0
Maximum Output Swing p-p [mA]	3.3	6.2

Signal to Noise Ratio	**0.18μm**	**0.13μm**
Signal to Noise Ratio at 1mA rms Output, 10MHz [dB]	79.50	88.57
Signal to Noise Ratio at 1mA rms Output, 100MHz [dB]	89.11	95.28
Signal to Noise Ratio at 1mA rms Output, 200MHz [dB]	94.26	98.06
Signal to Noise Ratio at 0.1mA rms Output, 10MHz [dB]	59.50	68.57
Signal to Noise Ratio at 0.1mA rms Output, 100MHz [dB]	69.11	75.28
Signal to Noise Ratio at 0.1mA rms Output, 200MHz [dB]	74.26	78.06
Dynamic Range	**0.18μm**	**0.13μm**
Dynamic Range at 100MHz [dB]	95.87	102.04
Fall and Rise Time	**0.18μm**	**0.13μm**
Fall Time 10%-90% at Input Step 1μA [ns]	3.31	1.84
Fall Time 10%-90% at Input Step 10μA [ns]	3.67	1.86
Rise Time 10%-90% at Input Step 1μA [ns]	3.29	1.83
Rise Time 10%-90% at Input Step 10μA [ns]	3.57	1.79
Noise Analysis	**0.18μm**	**0.13μm**
Total Input Referred Noise at 10MHz [pV/sqrt(Hz)]	270.92	143.97
Total Input Referred Noise at 100MHz [pV/sqrt(Hz)]	121.56	74.98
Total Input Referred Noise at 200MHz [pV/sqrt(Hz)]	102.44	68.93
Equivalent Output Noise at 10MHz [nV/sqrt(Hz)]	105.98	37.30
Equivalent Output Noise at 100MHz [nV/sqrt(Hz)]	35.05	17.22
Equivalent Output Noise at 200MHz [nV/sqrt(Hz)]	19.37	12.50

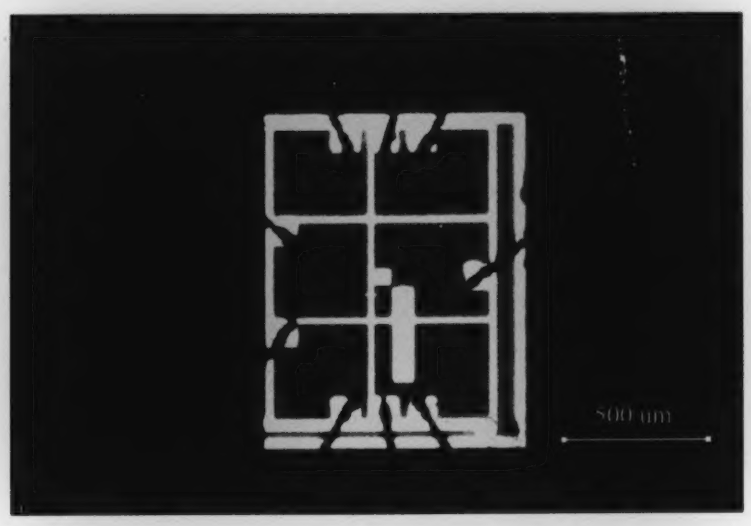


Figure 5.12: Prototype 5 - microphotograph of the sensor design

Table 5.5: CUT Average Power Supply Degradation

CUT Average Supply Current I_{DD} **[μA]**	**0.18 μm Design PSD [%]**	**0.13 μm Design PSD [%]**
100	0.28	0.41
200	0.56	0.83
300	0.83	1.25
400	1.11	1.67
500	1.39	2.08

Power dissipation of the 0.13 μm scaled design decreases by 13%. The design in 0.13 μm dissipates 5.7 mW whereas the design in 0.18 μm consumes 6.5 mW total power. The total silicon area of both designs remains approximately the same because most of the silicon is occupied by the pads. The core areas of the designs implemented in 0.13 μm and 0.18 μm technologies are 130 μm x 90 μm and 130 μm x 80 μm, respectively.

In the following, we show some results pertaining to 0.13 μm and 0.18 μm realization. Figure 5.9 and Figure 5.10 display how the DC transfer characteristic

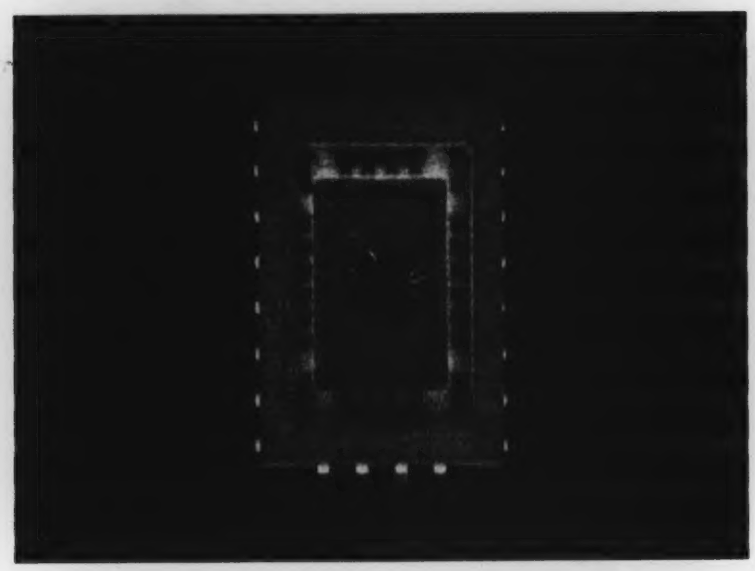


Figure 5.13: Prototype 5 - photograph of the sensor chip in 24-pin ceramic flat package

and frequency response of the amplifiers vary with the output biasing current I_{bias} (due to the limited variation of I_{bias}, the linear vertical scale is more representative). Figure 5.15 and Figure 5.16 show DC input-output current transfer characteristics of the 0.18 μm and 0.13 μm amplifier designs, respectively. It can be seen that the linear range and amplifier's gain are both increasing with increased I_{bias} current.

The amplifier's gain frequency characteristic is significantly improved with scaling. The improvement is measured in time domain with respect to the rise and fall time, and in the frequency domain with respect to the 3 dB bandwidth and unity gain frequency. Almost 100% improvement has been recorded for each parameter. The unity gain frequency extends to 6.8 GHz, whereas the 3 dB bandwidth is 190 MHz for the 0.13 μm design. For comparison with the 0.18 μm design, the reader is referred to Table 5.4.

The time domain response is demonstrated in the experimental simulation of typical monitoring application (Figure 5.17). This figure is intended to show the operational limits of the sensor. The power supply current of the monitored system

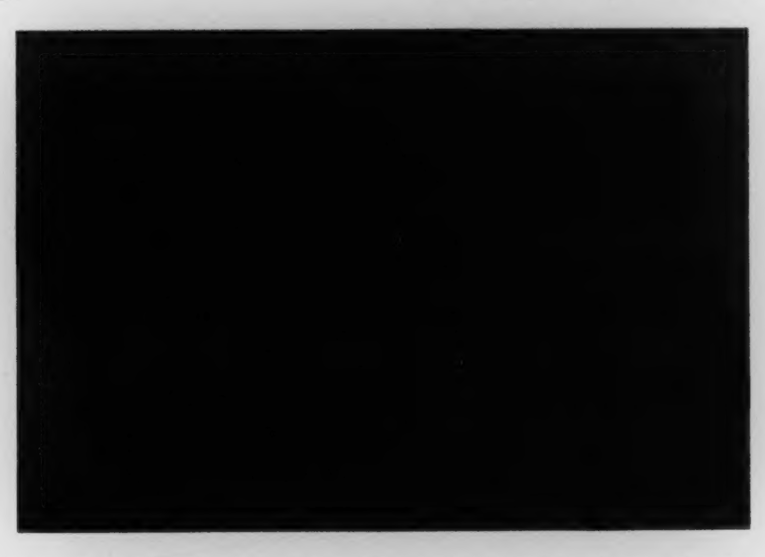


Figure 5.14: Prototype 5 - microphotograph of the sensor's core circuitry

with its high transient and small quiescent component is simulated at the input of the amplifier, at the frequency of 200 MHz. A static value of I_{DD} current of the system is set to 20 μA, and in one of the periods it linearly changes from 20 to 21.2 μA in steps of 200 nA. Even in the presence of high transients, the parametric analysis shows that the 0.13 μm monitor detects I_{DDQ} variations of 200 nA with observable output changes.

Total harmonic distortion (THD) is a measure of amplifier's linearity. In monitoring applications, the pass/fail decision sometimes requires the comparison of values within several microamperes range. This decision could be impaired with non-linearities of the amplifier. The THD of the 0.13 μm design has been improved with respect to 0.18 μm design. However, the reduced linearity distortion could not be attributed to the scaling process itself, but rather to a larger input swing of 30 μA for the 0.13 μm design obtained for the lower power dissipation. The relatively small input swing range doesn't limit successful application of the amplifier in either I_{DDQ} digital test applications or power supply current monitoring for analog circuits, I_{DD}. For the 0.13 μm design, the result of Discrete Fourier Transform analysis of the output current is shown on Figure 5.18. The circuit is excited with

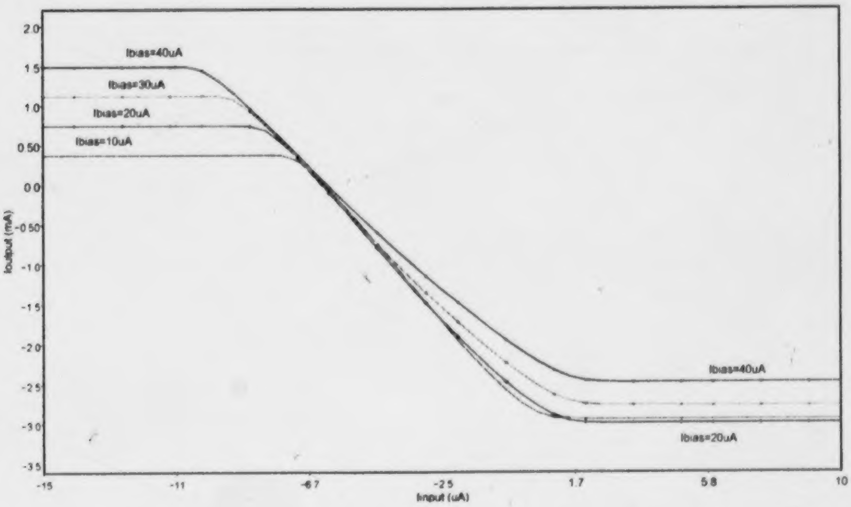


Figure 5.15: 0.18 μm amplifier DC current transfer characteristics for different I_{bias}

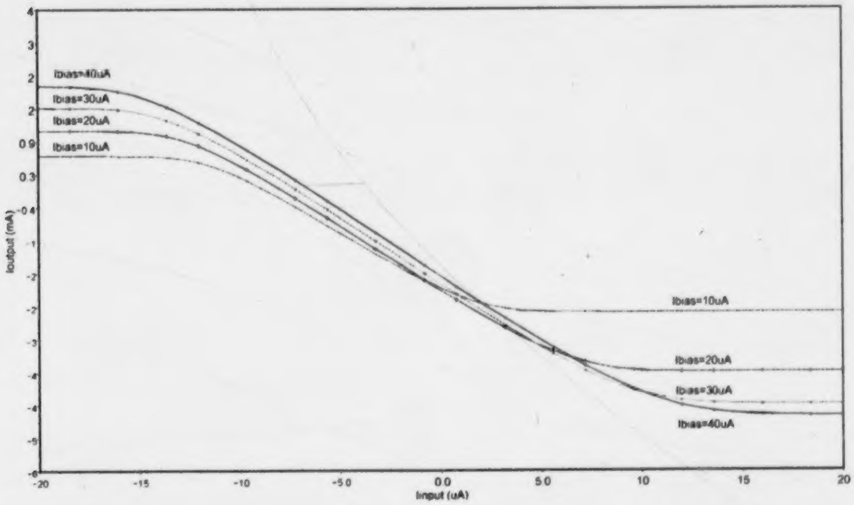


Figure 5.16: 0.13 μm amplifier DC Current transfer characteristics for different I_{bias}

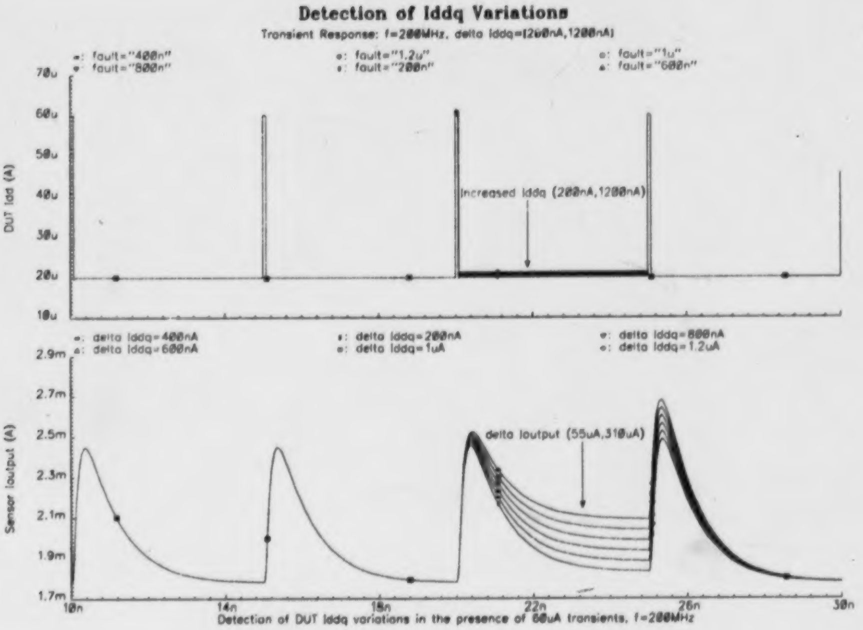


Figure 5.17: Detection of I_{DD} Variations

a 100 MHz sinusoidal input current with an amplitude of 1 μA. The analysis of the output signal shows that the second-order harmonic at 200 MHz is 55.9 dB lower then the main one. Other higher harmonics are even more suppressed, and this results in a low level of the total harmonic distortion. As one can see in Table 5.4, total harmonic distortion of the 4 μA peak-to-peak sinusoidal input signal is 0.3% for the 0.13 μm design.

Although the amplifier is placed in the power supply line of the monitored circuit, the level of the power supply degradation (PSD) during application is negligible. Since the sensing element R_S remained unchanged, the absolute level of degradation for both designs remained unchanged too. However, the relative power supply degradation for the 0.13 μm amplifier increases because the same voltage drop on R_S presents a higher percentage for the lower 1.2 V supply voltage. Details of the average power supply degradation could be found in Table 5.5 which gives experimental values of PSD levels for circuits whose supply current is simulated by

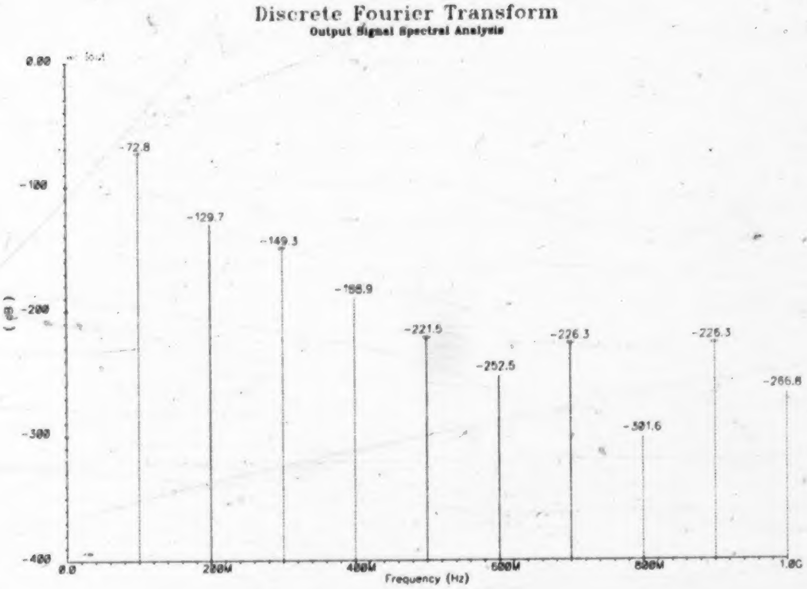


Figure 5.18: Discrete Fourier Transform of the output signal

the DC current source. More detailed power supply degradation analysis is given in Chapter 6, Subsection 6.3.2 on page 131. It is important to note that monitoring of the circuits that draw more then 500 μA requires only that one parameter of the amplifier be adjusted, that is I_{DC} input offset current. By this adjustment, the level of the power supply degradation can be substantially decreased and practically kept to the minimum. In application with digital circuits, the power supply degradation would be determined by the transient currents only. In other words, transient's average contribution to the total leakage current would be the only factor which influences the average power supply degradation.

The amplifier's high sensitivity performance is an important requirement for the efficient application in the monitoring scheme. Different sources of undesirable electrical interferences could mask a useful signal and make it indiscernible by the amplifier. To be detectable, the input signal must be higher then the noise floor

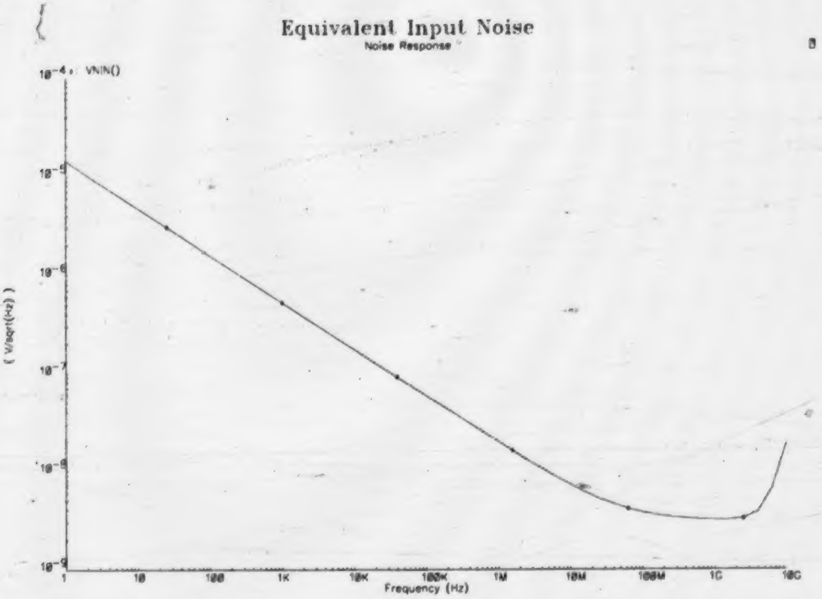


Figure 5.19: Input referred noise

of the amplifier. A minimum detectable signal is determined by the noise figure of the amplifier. The spectral density of the 0.13 μm amplifier's input referred noise is shown in Figure 5.19. To avoid the influence of flicker noise, we assumed the operation in the 100 MHz to 1 GHz range and calculated the spot noise over frequencies in this bandwidth. Yet, to have a better description of noise properties, we included the signal-to-noise ratio at low frequencies as well. The results of noise calculations are also summarized in Table 5.4. The largest source of noise is the source follower transistor in the input stage of the monitor. It contributes 30% to the total output noise. Nevertheless, the 0.13 μm design's signal-to-noise ratio of 75 dB for 0.1 mA 100 MHz output signal is reasonably high.

5.6 Conclusion

A novel application-specific high-frequency low-voltage current sensor amplifier has been proposed. Amplifier's topology is intended for power supply current monitoring applications. Due to its properties, the amplifier is suitable for I_{DDQ} test of digital circuits or power supply current monitoring of analog devices. Also, the impact of technology scaling on the amplifier's performance has been investigated. The proposed amplifiers have been implemented in 0.13 μm and 0.18 μm CMOS technology processes with 1.2 V and 1.8 V power supply voltage, respectively. Due to its overall performance, the amplifier has a strong potential for implementation with analog, digital and mixed-signal cores in system-on-chip monitoring applications. The scaling required no changes in the design topology, and resulted in the performance improvement. We expect that further scaling below 1 V will not require significant changes in the monitor architecture.

Chapter 6

Current Sensor in Digital Test Applications

6.1 Introduction

The evolution of the system-level integration has reached unprecedented dimensions. As projected by the 2001 Technology Roadmap, in the next 10 to 15 years we will see a system-on-chip (SoC) with several hundreds of embedded components that used to be individual VLSI devices [2]. Environments with such a magnitude of complexity require testing methodologies with significantly enhanced capabilities and test mechanisms which provide low-cost and high reliability verification solutions [27].

Evident difficulties in the defect identification process could be attributed to several factors. The concentration of the manufacturing defects is significantly increasing with every new, scaled technology. Shorts and opens are the major type of defects in integrated circuits. Dominant failure mechanisms very often manifest themselves as non-catastrophic faults. These kinds of faults (*e.g.*, resistive bridges, conductive opens) do not necessarily affect circuit's function and are usually not detected during the initial production testing. However, they can cause a malfunction very early in the product's life cycle and, as such, pose a significant reliability risk. Burn-in (Chapter 2, Subsection 2.2.3, page 11) is the standard approach to better expose such faults, but the method itself is becoming cost prohibitive. Since these faults cannot be fully described by the existing stuck-at-fault model, voltage-based

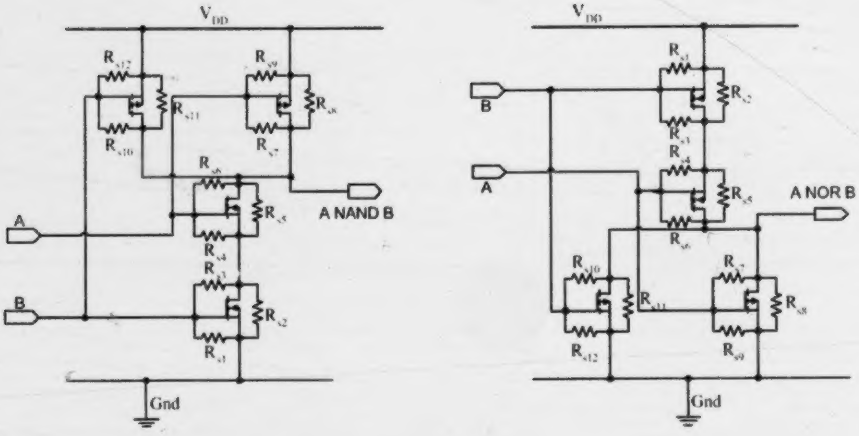


Figure 6.1: NAND and NOR gate resistive short faults

test techniques have a limited impact on their detection. Conventional methods provide only partial solutions to this problem, and are becoming severely limited by the strict power, area, and cost constraints. Therefore, new and improved techniques that would enable successful detection of such faults are needed.

Current monitoring has proved to be very effective in detection of these faults. It is widely used in the industry as a complementary test method, mostly as I_{DDQ} test. During today's production testing, I_{DDQ} test is performed on the entire chip by either the automatic test equipment (ATE) or an off-chip current sensor. Such approaches result in low testing speed, reduced sensitivity, and limited accuracy. Also, with the increasing number of integrated components, the reduced access to deeply embedded parts obstructs the controllability and observability of the testing process. Built-in current sensing devices could be a part of the solution which addresses these problems. Moreover, on-chip sensors could provide better information about a location of the fault because the sensor measures the supply current of a single embedded component or a cluster of embedded modules instead of the entire integrated circuit.

6.2 Digital Circuit Monitoring Application

In this chapter, we investigate feasibility, scope, and limitations of the current test technique for digital circuits based on the proposed built-in current sensing device which was presented in Chapter 5. A novel sensor topology is successfully employed in a current monitoring testing scheme. For verification purposes, the performances of the 0.13 μm design are investigated on several types of digital circuits: 64-bit RCA adder, 16-bit register, and inverter chain. The following experimental analysis is designed to probe sensor's detection capabilities of non-catastrophic short and open defects. Overall performance penalty and power supply degradation of the circuit under test are evaluated on 1.2 V 500-gate, 1000-gate, and 2000-gate asynchronous digital logic.

6.2.1 Context of Previous Work

The figures of merit for the successful current sensor design are outlined in Chapter 4, Section 4.2 on page 68. On the other hand, major contributions in the area of current sensor design have been described in Section 4.6 on page 77. Notably, most of the proposed sensor designs have been implemented in older technologies which do not reflect the same magnitude of secondary effects as VDSM processes. As mentioned before, the most significant impediment to effective employment of the BICS is the performance degradation of the circuit under test. The reported voltage supply degradation of 0.2-0.5 V for majority of the proposed 3.5 V or 5 V designs would not be acceptable in 1-2 V environment.

Beside detailed analog behavior analysis on which we elaborated in the previous chapter, ultimate performance of the proposed sensor needs to be verified in the current monitoring test application. For that purpose, we explore two key figures for sensor evaluation, that is, fault coverage and CUT performance degradation.

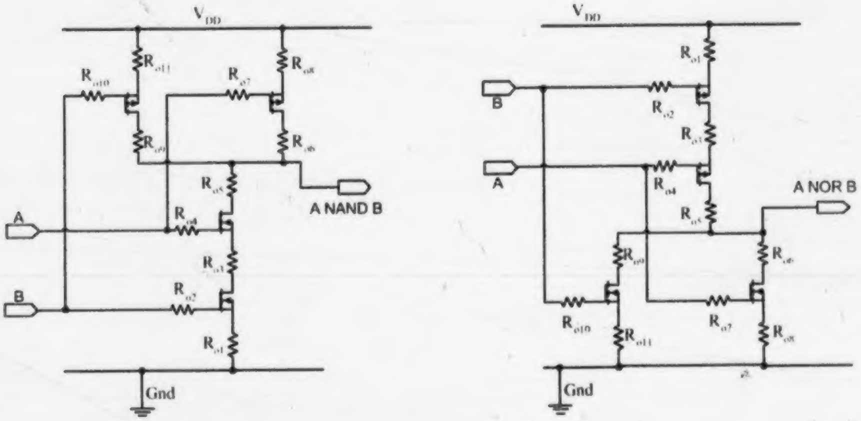


Figure 6.2: NAND and NOR gate conductive open faults

6.3 Experimental Simulations

The functionality and performance of the current sensor shown in Figure 5.2 on page 98 have been analyzed in a current testing monitoring scheme through a two-step experimental process. The first part of the experiment was intended to examine the fault coverage, sensor's capabilities, and limitations in detecting resistive open and short defects. The second part was designed to evaluate performance degradation of digital circuits of different complexity tested by this device. Two separate sets of test circuits have been designed for fault coverage and performance degradation evaluation purposes.

6.3.1 Fault Coverage

Catastrophic (hard) defects such as low-resistive path between two circuit's nodes are relatively easy to detect either through functional or parametric test. Detection of more subtle ohmic defects that do not necessarily cause functional faults has been a more challenging task. We investigated sensitivity of the proposed sensor in screening such defects.

Figure 6.1 and Figure 6.2 describe the set of resistive open and short defects within the NAND and NOR gates that were considered in this experiment. The

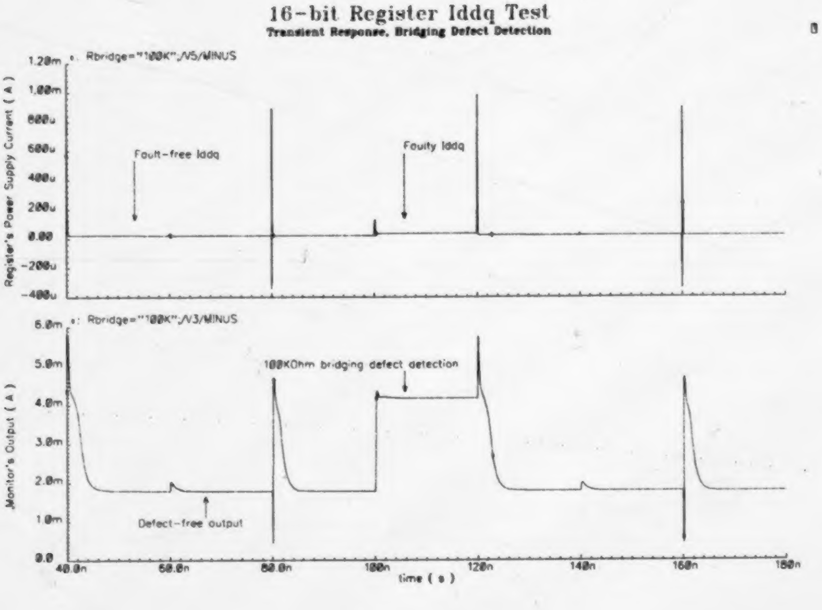


Figure 6.3: Resistive short defect detection, 16-bit register

complete set of all possible resistive shorts to be considered is very large even for circuits with a small number of gates. However, statistical probability of the faulty interconnect between two points is strongly dependent on their location and distance in the circuit layout. Therefore, we restricted our study to single resistive defects within the logic gate, and between the gate, source, and drain of the MOSFET device. Such resistive defects cause broken wires (opens) and bridges (shorts) in the circuit and are sometimes referred to as defect-oriented or physical faults [165], [18].

For the fault coverage analysis, a simulation experiment was conducted with samples of several types of digital circuits designed in 0.13 μm standard CMOS with a 1.2 V power supply. We used a 64-bit ripple carry adder (RCA) using 2-input standard CMOS NAND-gate logic, 16-bit register based on 1-bit clocked D-latch built with 2-input standard CMOS NOR-gate logic, and a simple chain of 100

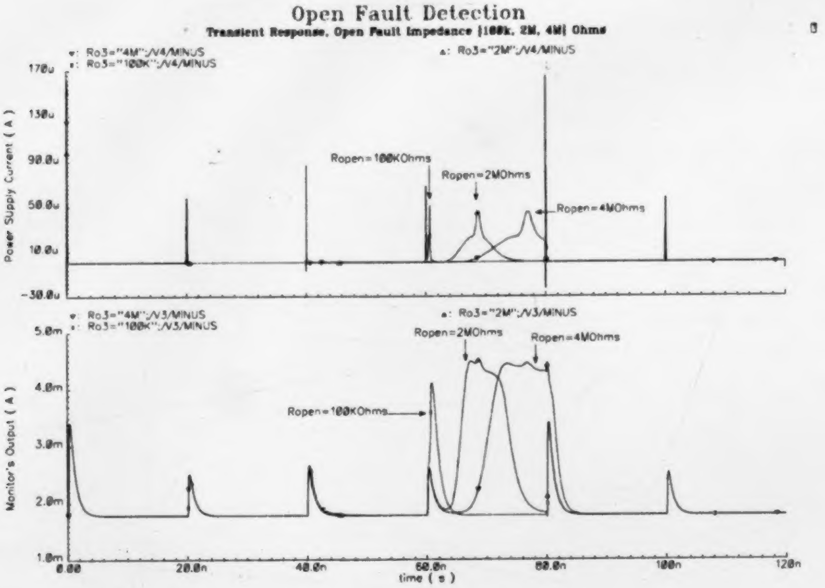


Figure 6.4: Conductive open defect detection, 16-bit register

CMOS inverters. Each circuit was connected to the sensor as a CUT in the current testing monitoring scheme shown in Figure 5.2. The logic was provided with a power supply through the sensing resistor.

All resistive defects from Figure 6.1 and Figure 6.2 have been implanted within different gates in the layout of the testing circuit. The resistances of defects were in the [0, 1G]Ω range, where 0 Ω bridge or 1 GΩ open presents a catastrophic defect. Although the fault coverage term is not defined for fault models with an infinite number of faults (*i.e.*, short or open resistance could have any value), we are using this term to quantify the efficiency of the sensor in terms of detectability of the minimum resistive open and maximum resistive short.

To be detectable, faulty current of a CUT has to be distinguishable from the normal variations of I_{DDQ} current. We also need to set an I_{DDQ} or ΔI_{DDQ} threshold which is known to be dependent on the fault-free leakage current level. Since the

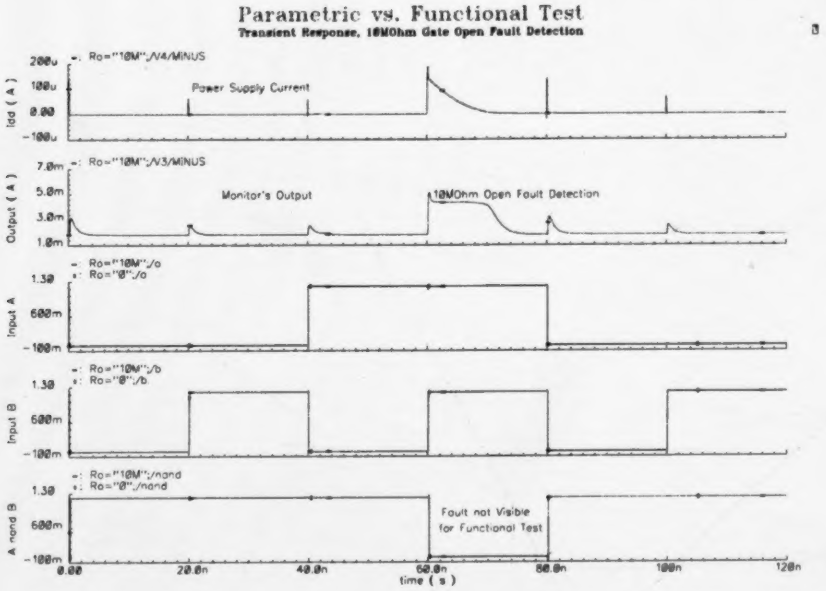


Figure 6.5: Conductive open defect detection, RCA adder

fault-free leakage current is a function of many variables which values have high variations and uncertainty, the faulty current can be either masked with them or wrongly reported in the case of a inappropriately set threshold level. For smaller circuits this threshold is set to the level at least one order of magnitude higher then the fault-free circuit, *i.e.*, ten times I_{DDQ}. For large circuits, the same approach would mean unacceptably high threshold level which would impair I_{DDQ} test as a screening tool and many faults would escape the test. Therefore, the threshold level has to be set accordingly so that it takes into account state dependent variations of the leakage current, process variations, and temperature.

Furthermore, the faulty current should be detected by the sensor, which is, in essence, an analog circuit characterized by a limited gain, nonlinearity, input and output referred noise, and output variations due to the process tolerances, mismatch, temperature, power supply noise, *etc*.. As we are probing sensor's limitations rather

Table 6.1: Sensor's Effect on I_{DDT} Current

500-Gate Logic	**Free Logic**	**Monitored Logic**	**Reduction [%]**
I_{DDT1} [mA]	1.478	1.030	**30.31**
I_{DDT2} [mA]	0.808	0.595	**26.41**
I_{DDT3} [mA]	1.353	1.022	**24.46**
I_{DDT4} [mA]	0.807	0.587	**27.22**
I_{DDT5} [mA]	1.476	1.028	**30.35**
Average [mA]	**1.18**	**0.85**	**27.75**

1000-Gate Logic	**Free Logic**	**Monitored Logic**	**Reduction [%]**
I_{DDT1} [mA]	4.502	2.316	**48.56**
I_{DDT2} [mA]	3.464	1.893	**45.35**
I_{DDT3} [mA]	4.022	2.167	**46.12**
I_{DDT4} [mA]	3.464	1.892	**45.38**
I_{DDT5} [mA]	4.526	2.324	**48.65**
Average [mA]	**3.996**	**2.118**	**46.81**

2000-Gate Logic	**Free Logic**	**Monitored Logic**	**Reduction [%]**
I_{DDT1} [mA]	10.871	3.839	**64.69**
I_{DDT2} [mA]	8.149	3.043	**62.66**
I_{DDT3} [mA]	9.782	3.618	**63.01**
I_{DDT4} [mA]	8.152	3.042	**62.68**
I_{DDT5} [mA]	10.923	3.843	**64.82**
Average [mA]	**9.575**	**3.477**	**63.57**

then I_{DDQ} test methodology itself, a designation of the detectable/non-detectable resistive defect from sensor's perspective is one of our primary objectives. For that reason, it is desirable to determine a minimum detectable signal (MDS) of the sensor. The MDS, which is dependent on the measurement bandwidth, is the smallest signal that can be detected above the noise. The level of the incoming signal which can be detected by the sensor pertains to the noise floor of the system. Table 5.4 in Chapter 5 provides details on sensor's input and output referred noise at several frequencies.

Table 6.2: Signal Delay between Test and Normal Mode of Operation

500-Gate Logic	50 Gates Delay [ps]	100 Gates Delay [ps]	200 Gates Delay [ps]
@ I_{DDT1}	29.41	51.77	81.69
@ I_{DDT2}	18.64	33.19	53.55
@ I_{DDT3}	29.54	51.96	81.64
@ I_{DDT4}	18.63	33.19	53.58
@ I_{DDT5}	29.40	51.77	81.61
Average Delay [ps]	**25.12**	**44.38**	**70.38**

1000-Gate Logic	50 Gates Delay [ps]	100 Gates Delay [ps]	200 Gates Delay [ps]
@ I_{DDT1}	79.05	133.88	200.27
@ I_{DDT2}	59.61	100.49	144.66
@ I_{DDT3}	69.05	117.31	171.96
@ I_{DDT4}	59.62	100.47	144.67
@ I_{DDT5}	79.06	133.67	199.86
Average Delay [ps]	**69.28**	**117.17**	**172.29**

2000-Gate Logic	50 Gates Delay [ps]	100 Gates Delay [ps]	200 Gates Delay [ps]
@ I_{DDT1}	161.14	282.15	427.78
@ I_{DDT2}	118.79	205.08	296.89
@ I_{DDT3}	143.88	252.00	374.70
@ I_{DDT4}	118.75	205.01	296.85
@ I_{DDT5}	161.27	281.93	427.31
Average Delay [ps]	**140.77**	**245.23**	**364.71**

Based on the sensor's noise figure, measurement bandwidth of 10-100 MHz, and minimum required signal-to-noise ratio at the input of 3 dB, we estimated a minimum detectable signal of ΔI_{IN}=[350, 500]nA at the input of the sensor. Taking into account 1.2 V supply voltage, the resistance of the maximum detectable short defect is calculated to be in the vicinity of 2-3 MΩ. In other words, any resistive short defect in the range 0-3 MΩ will be detected provided that the input test pattern activates a faulty path. Clearly, the detection of short defects with resistances in the lower end of this range will be more visible than the ones in the higher end. According to the study in [158], vast majority of bridging shorts have resistance of less then 20 kΩ, which is significantly lower than our detectability threshold of 3 MΩ. This makes them clearly detectable by the sensor.

Throughout our experiment, we confirmed that all shorts (Figure 6.1) within the 0-3 MΩ range were detectable. Indeed, appropriate input signals to the gate have to be supplied in order to make a fault visible. Figure 6.3 displays apparent detection of the short defect in a 16-bit register. The resistive defect R_{s4}=100 kΩ has been implanted in one of the NOR gates of the register. To expose the defect, combination of input signals $A = 0$, $B = 0$ is applied to the faulty gate. When the faulty path is activated, output of the sensor clearly detects elevated supply current.

The analysis of the open defects, Figure 6.2, was noticeably different. Open resistive defects mainly cause so-called delay faults. They affect the shape of the transient current and appear as delayed peaks of the power supply current. In Figure 6.4, when activated, a resistive faulty line of the 64-bit RCA adder manifests itself as a delayed transient whose peak and displacement are proportional to the open defect conductance. The open defect with resistance of 4 MΩ is clearly more visible then 2 MΩ open defect. Depending on the frequency, this kind of defect might not affect the logical level if the circuit's frequency is sufficiently low. Figure 6.5 displays RCA's power supply current, sensor's output, two NAND gate inputs, and NAND output. The implanted open defect produces time constant of the faulty RC network which is sufficiently low not to affect the logic level of the faulty NAND gate. It can be seen that this defect is practically invisible for functional test at 20 MHz test frequency. Nevertheless, the defect is clearly detected by the sensor through the parametric I_{DD} test.

The sensor was the most efficient in detection of resistive opens within the range of [100k, 50M]Ω at 20 MHz. This range is frequency correlated as it depends on the testing speed. Also, catastrophic opens with resistance approaching infinity were not visible with this sensor device. However, such defects are easily detectable by the functional test. Transparency of conductive open defects may be obscured sometimes, and such defects could be detected only by applying appropriate sequence to the input of the faulty gate. For example, in order to screen R_{O6} in NAND gate from Figure 6.2, one has to keep input A at '1' and then change input B from '1' to '0'.

6.3.2 Performance Degradation Analysis

The sensor is placed in the power supply line of a circuit under test. The sensing element is a 50 Ω resistor. Current which flows through the power supply line produces a small but measurable voltage drop across this resistor. This inevitably results in the power supply degradation (PSD) and, consequently, performance decline. The following analysis is intended to quantify the actual performance penalty due to the sensing element. Setting a higher value of the resistor yields more sensitivity, but negatively impacts performance of the circuit under test. On the other hand, very small resistor produces less degradation, but, unfortunately, diminishes sensor's capacity to screen low resistive opens and high resistive shorts.

In our next experiment, we observed performance degradation of digital circuits of different complexity. The higher number of logic gates leads not only to the higher level of static leakage current, but also to more intensive switching activity and proportionally higher transients. With the sensing element in the power supply line, transients could severely affect operation of the circuit under test.

We used three samples of asynchronous, combinational, standard CMOS digital logic with 500, 1000, and 2000 gates designed in a standard 0.13 μm CMOS process with a nominal power supply of 1.2 V. The selection of circuits for this analysis was based on the following criteria: 1) The sensor is evaluated in testing of standard CMOS circuits and, therefore, a CUT must be a digital circuit realized in standard CMOS logic; 2) Performance degradation will be mainly affected by the level of switching transients, which are directly proportional to the complexity/size of the CUT (assuming that the frequency of switching and power supply voltage are fixed parameters). Having in mind 1) and 2), it is clear that, for example, a function of the circuit (*e.g.*, adder, multiplier, ...) is not relevant for this evaluation. It is also clear that the way the digital function is realized (NOR gates, NAND gates,...) is of secondary importance.

With each circuit we did a following experiment: one sample of the logic was connected to the power supply directly, and the other, identical one, was connected to the power supply through the sensing device. We observed and compared several

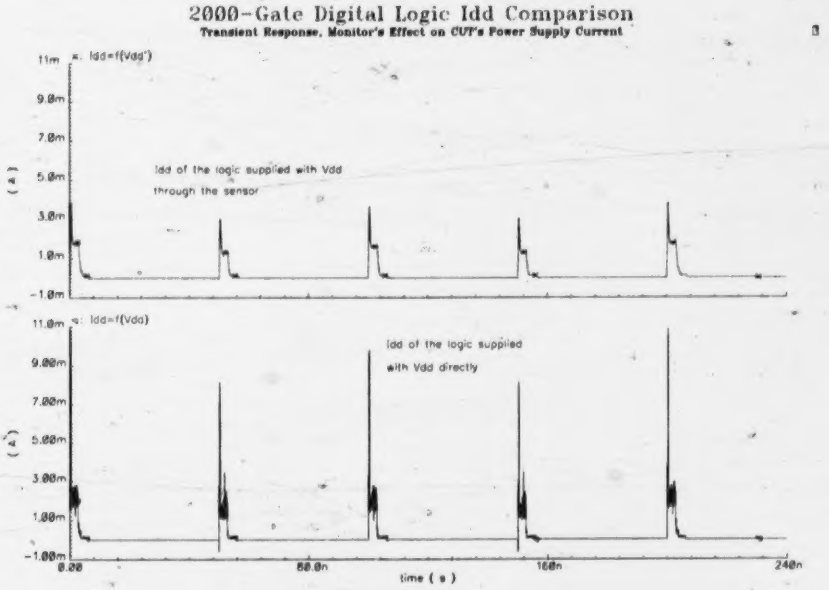


Figure 6.6: Suppressed transients in the presence of the sensor

key points in the operation of the logic under test: the sensor's effect on transient currents, resulting delay between corresponding output signals with respect to the number of gates through which signal propagates, sensor's effect on average power consumption, and average power supply degradation.

From the input to the output of each logic sample, the signal propagates through identical 300 gates. Within the observed period of time (250 ns), all logic gates change the output state at least once. The highest recorded transient peak I_{DDT1} for each logic, Table 6.1, corresponds to the moment when all gates switch the state. The terms 'free logic' and 'monitored logic' in the table refer to the same logic without and with sensor device in its power supply line, respectively. As it can be seen from the table, higher the transient peak of the logic is, higher the percentage of its suppression by the sensor. For example, 10.92 mA transient I_{DDT5} (2000-gate logic) is reduced to 3.84 mA after passing through the sensing element. Reduced

Table 6.3: Average Power Dissipation and V_{DD} Degradation

500-Gate Logic	**Average Power [μW]**	**Average V_{DD} [V]**	**V_{DD} Degradation[%]**
Test Mode	32.77	1.198	**0.167**
Normal Mode	33.77	1.200	**0**

1000-Gate Logic	**Average Power [μW]**	**Average V_{DD} [V]**	**V_{DD} Degradation[%]**
Test Mode	72.69	1.196	**0.333**
Normal Mode	78.82	1.200	**0**

2000-Gate Logic	**Average Power [μW]**	**Average V_{DD} [V]**	**V_{DD} Degradation[%]**
Test Mode	142.91	1.193	**0.583**
Normal Mode	167.82	1.200	**0**

transient current converts to extended discharging time of the gate capacitance and, as a result, performance degradation. When the circuit is powered through the sensor, the peak of the transient current is reduced on average 28% for the circuit with 500 gates, 47% for the 1000-gate logic, and almost 64% for the 2000-gate logic. The actual values of reduction are listed in Table 6.1. This is also shown in time domain in Figure 6.6 which compares I_{DD} current of the 2000-gate logic in normal and test mode of operation.

Nominal I_{DDQ} quiescent current for a 1.2 V 0.13 μm device fabricated in standard CMOS process can be estimated anywhere between [0.001, 10]nA/μm and is mainly determined by the threshold voltage, V_{TH}, and the thickness of the gate oxide, t_{ox}. Total gate leakage will depend on factors such as: type of logic, transistor sizes, voltage supply, temperature, *etc.*. In our case, for all tested circuits, quiescent current comprise less than 10% of the total average power supply current at the switching frequency of 20 MHz. We noticed that this percentage decreases as complexity of the circuit increases. Consequently, by suppression of the transients, we can approximate that the total power supply current of the CUT is proportionally reduced, too. We also conclude that the actual PSD can not be accurately estimated based solely on independent analysis of the sensor and the circuit under test.

Delay between signals which propagate through the same path are observed after propagation through 50, 100, 200, and 300 logic gates. The delay is measured between the two corresponding transitions. One such example, for the 1000-gate logic, is shown in Figure 6.7. Here, the output signal of the monitored logic, which propagates through the critical path of 100 gates, is delayed from the same signal of the 'free logic' for 117 ps. Detailed results for all three test circuits are listed in Table 6.2. As expected, transients with higher peaks introduced more delay between the signals. Figure 6.8 summarizes delay analysis for the three digital circuits. It provides a reference as to what kind of performance penalty one might expect when testing a logic with the given number of gates and the length of the critical path. For example, a 500-gate digital logic with a critical path of 200 gates tested for I_{DDQ} at 20 MHz will have an average output signal delayed by approximately 70 ps. Actual figure may vary depending on the gate's transistor sizes.

Summary of the average power consumption and V_{DD} degradation for all three CUTs tested at 20 MHz are shown in Table 6.3. High transients are undoubtedly the main contributor to the power supply degradation and performances deterioration. By introducing the extra series device to the power supply, a logic will incur a performance penalty. However, the average PSD of less than 0.6% for the circuit with 2000 gates tested at 20 MHz is relatively negligible. The results from Table 6.3 could be further extrapolated for the circuits of higher complexity.

6.4 Discussion and Application Perspective

The presented sensor has proven to be a valuable testing tool. With its excellent frequency characteristic, small silicon area and reasonable power dissipation, this versatile built-in sensor device has a strong potential in detecting low-resistive open and high resistive short defects in digital circuits.

Implementation of the monitor as a built-in current sensor would clearly incur some performance penalty. To weigh how much of V_{DD} degradation will actually occur and to reduce potential implication, one has to consider many factors. Testing a high complexity digital circuit would require partitioning to smaller modules which would satisfy requirements regarding allowed performance degradation. To

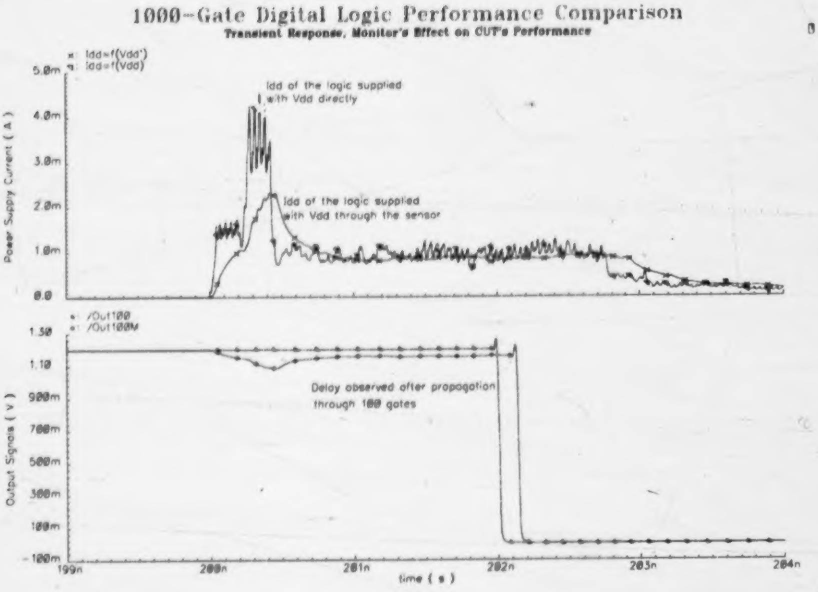


Figure 6.7: Delay between same signals after propagation through 100 gates

evaluate the size of partitions, several points have to be taken into account: logic type, transistor sizes, test frequency, estimated switching activity, the length of the critical path, nominal power supply, operating temperature, *etc.*.

By partitioning and increasing number of monitored logic modules, we also increase the overall power consumption. In order to reduce excessive consumption due to the BICS, the sensor could be adapted to operate in two modes: test and normal mode. The sensor would be active only during the test mode. In the normal mode, the device should be cut off from the rest of the logic, thus reducing additional power consumption and performance degradation to zero.

All figures in our work are given with respect to 1.2 V power supply, fixed temperature of 27 °C, and the test frequency of 20 MHz. The similar analysis with 1.8 V digital circuits and the 0.18 μm sensor shows somewhat better sensitivity of the monitor and, as expected, better PSD results [35]. This is mainly due to the

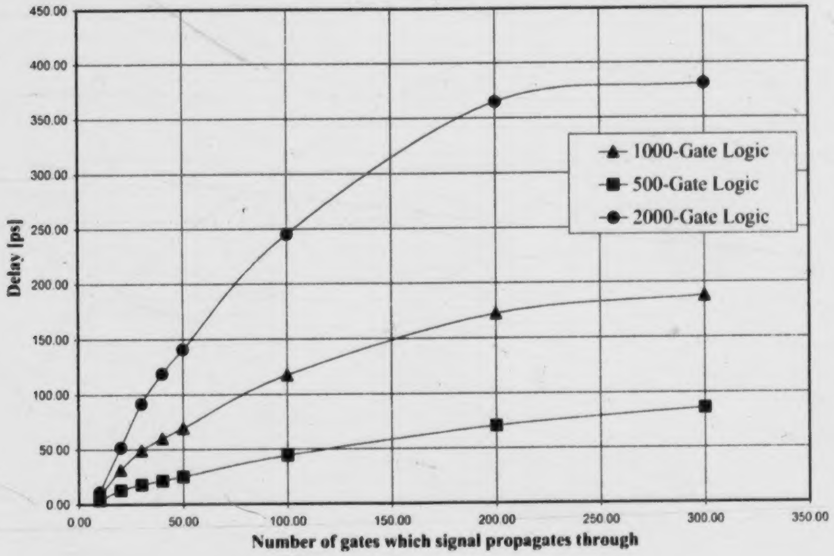


Figure 6.8: Delay between corresponding signals vs. length of critical path

fact that the sensing element remains unchanged so that the relative power supply degradation for the circuits with a built-in 0.18 μm sensor decreases. The same voltage drop across resistor R_S presents lower percentage for the higher, 1.8 V, supply voltage. On the other hand, the 0.13 μm design displayed better high-frequency properties.

6.5 Conclusion

A test application of the novel topology of the high-frequency current sensor has been presented. The sensor is designed for power supply current monitoring of digital circuits. The feasibility of practical implementation, overall resistive defect detection efficiency, and expected performance degradation has been the focus of this analysis. Acceptable performance penalty and high sensitivity have been demonstrated. The proposed sensor have been implemented in standard 0.13 μm and 0.18 μm CMOS technology processes with 1.2 V and 1.8 V power supply voltage, respectively. The sensor has potential for implementation with digital cores as a built- in I_{DDQ} current sensing device. The scaling required no change in the design topology and resulted in the apparent performance improvement. We expect that further scaling below 1 V will not require significant changes in the monitor architecture and, therefore, we propose it as a practical, versatile, and scalable built-in test solution.

(no text)

Chapter 7

Process Variations

7.1 Introduction

The aggressive scaling in manufacturing of integrated circuits (IC) which happened in the past is expected to continue in the near future. Projections from the International Technology Roadmap for Semiconductors (ITRS) show that by the year 2016, leading edge maximum-performance CMOS devices will have 9nm physical gate length and supply voltage of 0.4 V [181], [183]. Scaling undoubtedly improves the performance of the circuit but, on the other hand, has some detrimental effects, too. One of the undesirable consequences of device scaling is an increased impact of process variations on the circuit performance. Device behavior will become increasingly sensitive to variations in semiconductor processing as the technology is scaled downward [24]. When device dimensions are small, any variation can have a significant impact on performance.

As a result, predicting the effects of process variations on the performance of integrated circuits may become an important factor in the design flow. Moreover, circuit design and test techniques that can deal with variability and variation-tolerant circuit designs may be an alternative cost-effective way to counter rising process uncertainties. Such techniques are a complement to more advanced process techniques that reduce variability. Effect of process and parameter variations on MOSFET's current which is used as a tool for fault detection is explored in the following sections.

Table 7.1: Scaling Trends and Process Variations

Year	**1999**	**2001**	**2003**	**2006**	**2010**	**2016**
Technology Node[a]	**180 nm**	**130 nm**	**100 nm**	**70 nm**	**45 nm**	**22 nm**
$V_{DD}{}^{b}$ **[V]**	1.5–1.8	1.1–1.2	1.0–1.2	0.9–1.2	0.6–1.0	0.4–0.9
$3\sigma(V_{DD})$ **[%]**	±5	±5	±5	±5	±5	±5
$t_{ox}{}^{c}$ **[nm]**	3.5	2.3	2.0	1.9	1.2	0.9
$3\sigma(t_{ox})$ **[%]**	±4	±4	±4	±4	±4	±4
$V_{th}{}^{d}$ **[V]**	0.45	0.4	0.35	0.3	0.25	0.25
$3\sigma(V_{th})$ **[mV]**	48–55	33–42	27–36	18–27	15–25	15–25
$L_{gate}{}^{e}$ **[nm]**	140	90	65	40	25	13
$3\sigma(L_{gate})$ **[nm]**	14.0	6.31	4.46	2.81	1.77	0.88

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[a] Technology node is defined by the minimum half-pitch of custom-layout metal interconnect. For each node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

[b] Nominal voltage power supply

[c] Equivalent electrical oxide thickness

[d] Long channel threshold voltage

[e] L_{gate} denotes a length of the gate, as printed in photoresist. A physical gate length is smaller than the feature size printed in the resist.

7.2 Sources of Variations

Performances of integrated circuits are influenced by many factors. Generally, based on the source of their origin, all factors could fit into one of two groups: environmental or physical.

Deviation from circuit's expected behavior could be a result of changing the environment conditions in which the circuit operates. For instance, a change in temperature could affect electrical properties and characteristics of the MOSFET device (*e.g.*, mobility, threshold voltage,...), conductance of interconnects, resistance of passive elements, *etc*.. Consequently, these changes would affect the operation of the circuit as a whole. Such conditions as well as their manifestations are temporary in nature.

On the other hand, circuit's characteristic is strongly dependent on the physical implementation of its elements. In a complex manufacturing process, interconnects, active devices, passive elements are susceptible to the imperfections of the fabrication process. Interconnect variations play an important role in a complete variability analysis. As the scaling continues and complexity of circuit design increases, interconnect variation becomes one of the limiting factors of circuit performance [189]. Nevertheless, the most significant limiting factor of circuit performance is variation in MOSFET device parameters. In general, variation of the device could be attributed to the deviation of the following parameters:

- Geometry parameters (*e.g.*, gate oxide thickness, length, width,...);
- Material parameters (*e.g.*, doping, deposition, anneal[1],...);
- Electrical parameters (*e.g.*, threshold voltage, leakage currents,...).

In our study, we focus our attention on variations within a MOSFET device and its impact on transistor's output characteristics. Such deviations from nominal parameter values are permanent. The scaling trends and projected process tolerances of some of electrical and geometry parameters based on the ITRS publications [181], [182], [183] are given in Table 7.1.

7.3 Previous Research

Much research has been devoted to the analysis of the sources, historical trends, and modelling of process variations in the design process. In [15] and [129], the authors summarize the sources and trends in device and wire variability, and process characterization methodologies. The works stress the importance of design for variability methodologies in the presence of inter and intra-die process variations. Such design for variability techniques should be developed and integrated into existing and future design environments. The authors don't provide more detailed insight into different impact of process variations on various types of circuits, namely analog or digital. This impact is definitely different. For instance, the wire variability, undoubtedly important factor for digital circuits with large amount of interconnect, will have a smaller effect on analog circuits simply because of their size which usually have less then 100 transistors. On the other hand, analog circuits usually contain transistors with a wide variety of sizes, each of which has different susceptibility to process variation.

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[1] *Annealing* is the process in which silicon wafers are exposed to a heat treatment, so that dopant atoms (usually, boron, phosphorus, or arsenic) can be incorporated into substitutional positions in the crystal lattice, resulting in changes in the electrical properties of the semiconducting material.

In [190], Srivastava *et al.* described the impact of process variation on leakage power for 0.18 μm CMOS technology and showed that variability in a device length, L, channel dose, N_{sub}, and the gate oxide thickness, t_{ox}, could lead to substantial changes in V_{TH} and, consequently, drastically affect the leakage current. They confirmed empirically that the leakage current is exponentially proportional to the change of gate length and gate oxide thickness, but linear to the change in channel doping. In their experiment, they used a simple CMOS inverter and a NAND gate, and applied the logic signal to the input of the gate. Analysis of this kind is limited to the digital circuits only, and to leakage current of CMOS devices in the subthreshold region. As such, the analysis doesn't provide insight into the analog behavior of the device in the presence of variations, and the magnitude of this impact. The sensitivity analysis of analog circuits to process variation clearly requires a different approach. The impact of process variation on device's current in saturation and ohmic region should be a main concern of variability analysis for analog circuits.

Sato *et al.* characterized the effects of statistical process variation on the 0.35 μm CMOS performance [168]. They conducted the variation analysis for threshold voltage and saturation drain current and found that variation of the gate oxide formation has the most significant effect on the NMOS drain current. The authors limit their prediction of NMOS and PMOS device sensitivity to process variation to 0.25 μm CMOS process only. In the presence of the fast scaling trends, sensitivity analysis to process variation in more advanced CMOS processes such as 0.18 μm, 0.13 μm and below is needed.

In [170], Scheffer proposed less conservative, more realistic, explicit computation of performance as a function of process variations which allows better yield optimization in the design process. The author limits the scope of the paper to interconnect variations and their impact on timing analysis. Application of the same approach to the other sources of variations (*i.e.*, device parameter variations, *etc.*), which are more dominant in analog circuits, is questionable. Similarly, the authors in [189] restricted the analysis of circuit sensitivity to interconnect variations only.

Keshavarzi *et al.* [83] elaborated how barriers to technology scaling, such as leakage and parameter variations, challenge the effectiveness of current-based test techniques. They proposed a multi-parameter test approach which improves the current testing sensitivity. The authors investigated leakage in the context of frequency, temperature, and body-bias. However, the impact of the manufacturing process variations has not been explored.

Application of current-based techniques to analog circuits usually implies detection of faulty current when transistors in a circuit operate in different modes of operation. In such case, a contribution of the leakage currents described in Chapter 3, Section 3.4 to the total supply current is negligible.

7.4 Motivation and Problem Outline

In this part of our research work, we try to quantify absolute and relative deviation of the MOSFET's drain current from the nominal value based on the BSIM3v3 transistor model and estimated manufacturing parameter tolerances outlined in referenced ITRS documents [183], [182], [181], [178] and other publications [129], [190]. These deviations are given with respect to the size of the transistor, width-length aspect ratio, and V_{DS} and V_{GS} biasing voltages which determine the operation mode of the transistor.

The statistical variation of the N-type MOSFET drain current has been evaluated in three modes of operation: saturation, ohmic, and subthreshold conduction. The results could be used as a reference, for example, in current testing of analog circuits which uses the level of power supply current for defect screening.

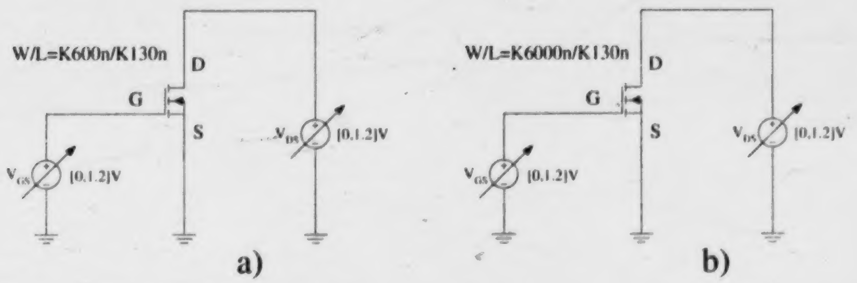

Figure 7.1: Experimental setup for transistors with constant aspect ratio
a) $W/L = K600$ nm/$K300$ nm b) $W/L = K6000$ nm/$K300$ nm

In Chapter 3, Section 3.3.4 on page 41, we surveyed proposed I_{DD} current-based test methods for analog circuits. In contrast to digital circuits, the transistors in analog circuits do not operate as simple switches. Evaluation of the drain current, which is not necessarily composed of the leakage components only, could have a major impact on the successful application of the current-based test to analog circuits. Being able to differentiate between process variation and faulty current has been a most challenging problem. This has certainly significant implication on analog current-based test.

7.5 Experimental Simulations

From designer's point of view, it is very important to know how the sizing of transistors influences process variation sensitivity of drain current. To determine the sensitivity to process variations, a simple experimental setup has been prepared. Figure 7.1 and Figure 7.2 display circuit's schematic used to evaluate the impact of process variations on transistor drain current for different transistor sizes and various biasing conditions. For each setup, we performed statistical analysis and investigated how the component variation affects the drain current.

With Monte-Carlo analysis, designers can verify whether their designs will be successful despite small changes in component values due to the manufacturing fluctuations. Monte-Carlo techniques for prediction of IC yield are well established

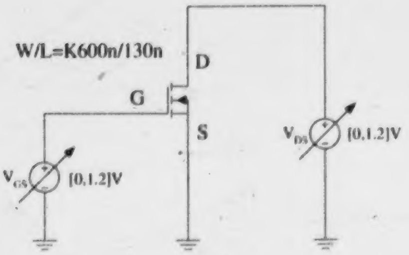

Figure 7.2: Experimental setup for transistors with variable aspect ratio $W/L = K \cdot 600$ nm/300 nm

Table 7.2: Standard Deviations of Varied Process Parameters

Parameter	BSIM3v3 Name	Standard Deviation σ
oxide thickness	tox_n	0.5e-10 m
intrinsic threshold voltage	$vtho_n$	0.01 V
mobility	μo	1.0e-3 m^2/Vs
width	W	1.5e-09 m
length	L	1.5e-09 m

in the literature, but their use in commercial design is limited by their high computational cost. The statistical analysis tool provides a quantitative measure on how the manufacturing variations in IC devices affect the production yield of a given design. The tool performs multiple simulations, with each simulation using different parameter values for the devices based upon the assigned statistical distributions.

Monte-Carlo analysis with 1000 runs for each V_{GS} and V_{DS} biasing point and for different $\frac{W}{L}$ aspect ratios has been performed. Table 7.2 shows BSIM3v3 model parameters varied in this experiment. The Gaussian distribution is assumed as the basic distribution for independent random variables. It is important to note that the variations in W and L are uncorrelated, as they are defined in different process steps: W - in the field oxide step, L - during the polysilicon definition and the source and drain diffusion processes. The experiment consists of two parts and they are described in the following paragraphs.

7.5.1 Constant W/L Aspect Ratio Simulation Results

The first part of the experiment analyzes the impact of process variations on NMOS transistors of different sizes with constant $\frac{W}{L}$ ratio, as shown in Figure 7.1. In this section we include the results for smaller size transistors $\frac{W}{L} = \frac{K\cdot 600n}{K\cdot 130n}$, and bigger transistors $\frac{W}{L} = \frac{K\cdot 6000n}{K\cdot 130n}$, where K represents a width-length dimension multiplier (K=1, 1.2, 1.4,...., 3.8, 4). Figures 7.3–7.11 (pages 147–149) display results for transistors with $\frac{W}{L} = \frac{K\cdot 600n}{K\cdot 130n}$ aspect ratio, three V_{GS} voltages (V_{GS}=0.6 V, V_{GS}=0.9 V, V_{GS}=1.2 V) and 16 width-length multiplication factors, *i.e.*, K=[1, 4] in steps of 0.2 increment. The aspect ratio of the transistors remain the same in this part of the experiment although the sizes of W and L change proportionally. For each V_{GS}, three graphs are shown with:

- mean value of drain current, $\bar{\mu}(I_D)$ [μA],
- standard deviation, $\sigma(I_D)$ [μA],
- relative standard deviation with respect to the mean value, $\frac{\sigma(I_D)}{\bar{\mu}(I_D)} \cdot 100[\%]$.

Each graph includes five curves for five different V_{DS} values (*i.e.*, V_{DS} = 0.3, 0.5, 0.7, 0.9, 1.1 V). Each curve shown on any of these graphs is a result of 16000 simulations which have been performed through Monte-Carlo statistical analysis.

In a similar fashion, Figures 7.12–7.20 (pages 150–152) show results for transistors with larger width dimensions, *i.e.*, $\frac{W}{L} = \frac{K\cdot 6000n}{K\cdot 130n}$, three V_{GS} voltages (0.6 V, 0.9 V, and 1.2 V), and factor K=[1, 4] in steps of 0.2 increment.

The first important observation of the Figure 7.3 and Figure 7.5 reveals that the percentage of the drain current relative deviation is strongly inversely proportional to the mean value of the drain current. When the curves showing drain current mean values $\bar{\mu}(I_D)$ decrease and reach their minimums (Figure 7.3), the curves showing the percentage (Figure 7.5) increase and reach their maximum peaks. This is valid for all V_{DS} values and for smaller as well as bigger size MOSFETs (*e.g.*, as shown in Figure 7.12 and Figure 7.14).

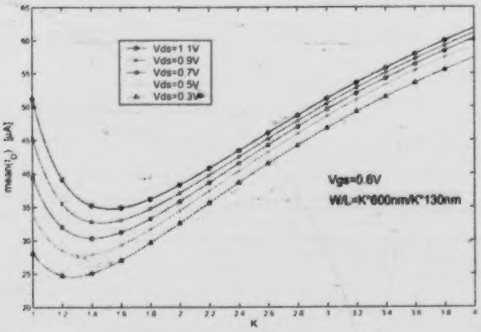

Figure 7.3: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

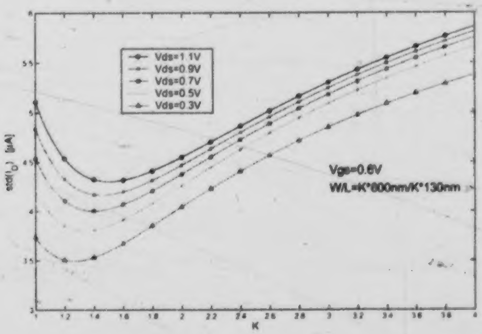

Figure 7.4: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

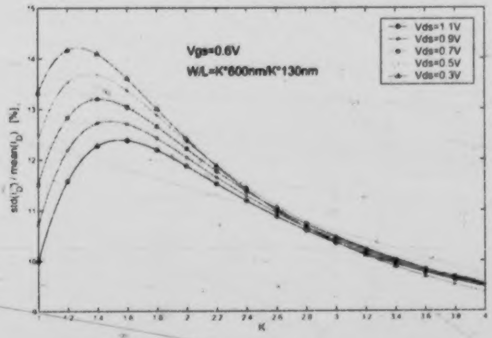

Figure 7.5: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

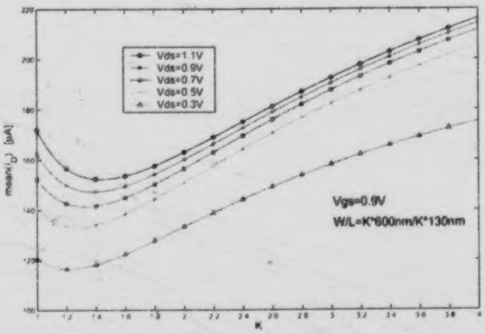

Figure 7.6: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

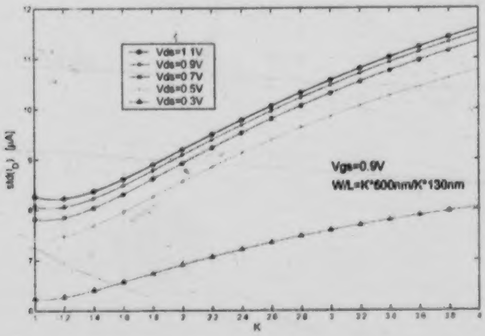

Figure 7.7: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

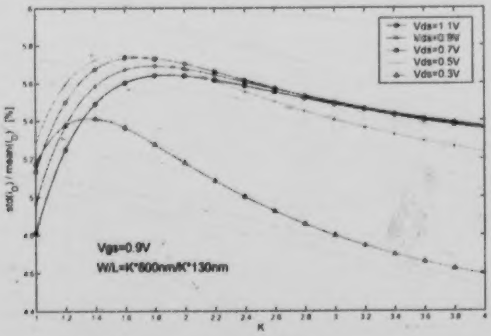

Figure 7.8: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

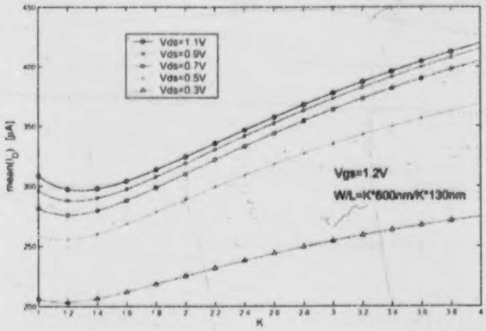

Figure 7.9: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}, V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

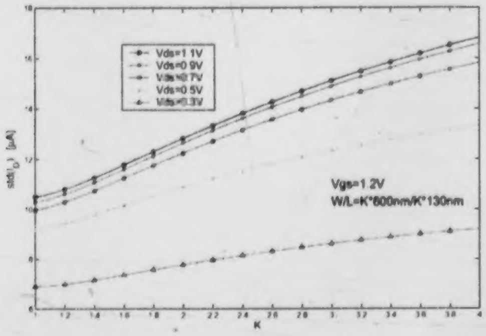

Figure 7.10: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}, V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

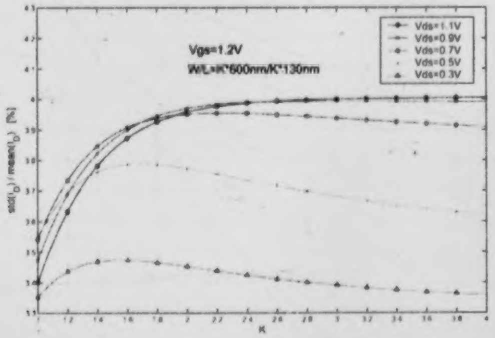

Figure 7.11: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}, V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 600\ nm}{K \cdot 130\ nm}$

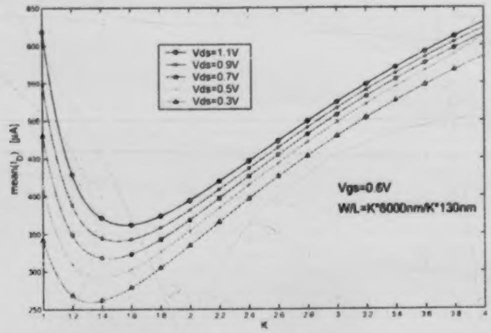

Figure 7.12: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

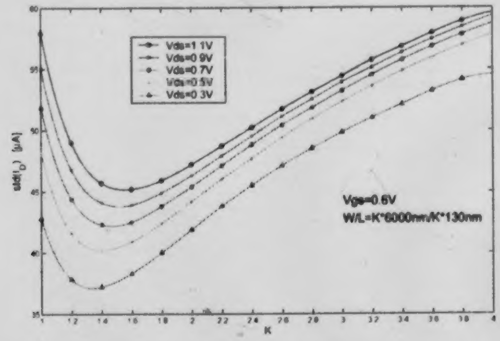

Figure 7.13: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

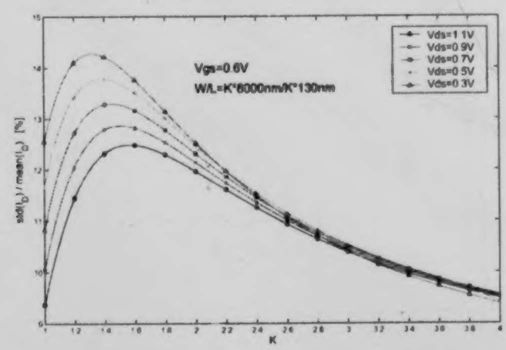

Figure 7.14: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}, V_{GS}=0.6 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

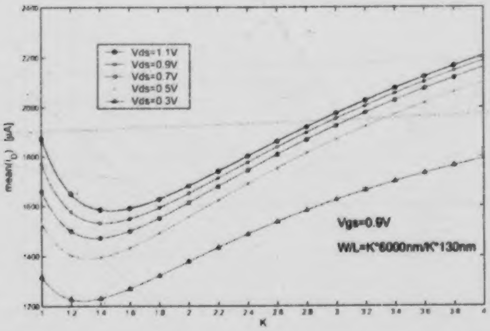

Figure 7.15: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

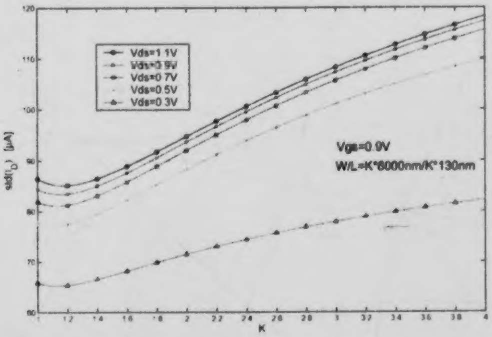

Figure 7.16: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

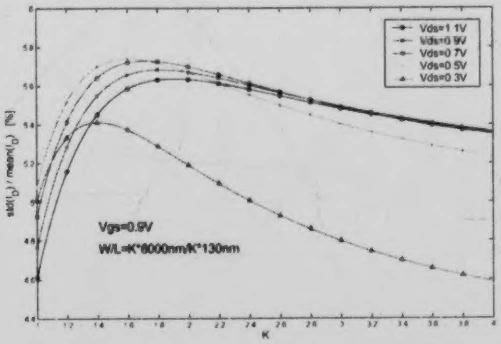

Figure 7.17: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}, V_{GS}=0.9 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

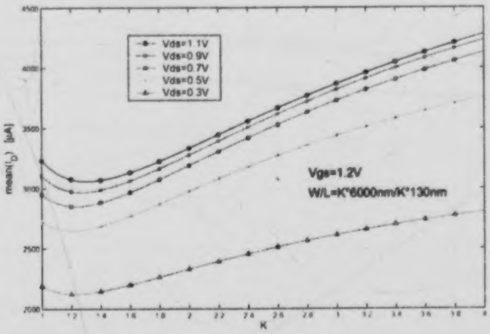

Figure 7.18: Drain current characterization of the MOSFET device with constant aspect ratio – I_D mean vs. K for different V_{DS}. V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

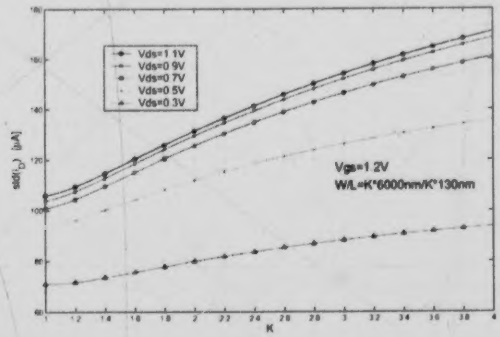

Figure 7.19: Drain current characterization of the MOSFET device with constant aspect ratio – I_D standard deviation vs. K for different V_{DS}. V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

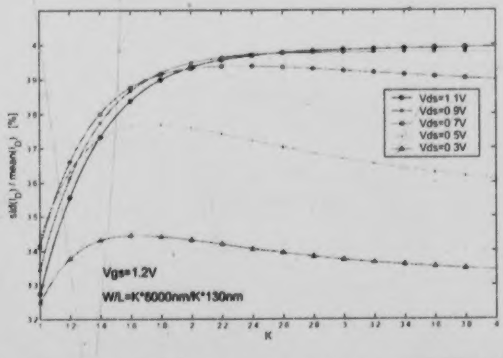

Figure 7.20: Drain current characterization of the MOSFET device with constant aspect ratio – Percentage of I_D variations vs. K for different V_{DS}. V_{GS}=1.2 V, and $\frac{W}{L} = \frac{K \cdot 6000\ nm}{K \cdot 130\ nm}$

Nevertheless, by comparing corresponding graphs in Figure 7.5 for smaller transistor and Figure 7.14 for bigger transistors and V_{GS}=0.6 V bias voltage, we notice that curves look almost identical with a swing of approximately 9.5%-14.3%. Similarly, almost identical swing of 4.5%-5.8% could be seen by comparing the graphs in Figure 7.8 and Figure 7.17, or 3.3%-4.1% by comparing Figure 7.11 and Figure 7.20. This indicates that there is no visible strong correlation between the width dimension of the transistor and process variations.

Under the same biasing condition, as it can be seen on graphs in Figure 7.5 and Figure 7.14, the mean values of the drain currents are directly proportional to the the ratios of transistor sizes, W/L. This, of course, doesn't come as a surprise. At the same time, an approximately equal percentage of the standard deviation for currents in both cases could be observed. In addition to our first observation, where we had a constant aspect ratio, this leads us to conclude that the length of the device could be a critical factor which determines sensitivity of the device to process variation.

7.5.2 Variable W/L Aspect Ratio Simulation Results

In this part of the experiment, a behavior of the device with a variable aspect ratio is simulated in a presence of the process variation. As shown in Figure 7.2, the aspect ratio of the transistors is $\frac{W}{L} = \frac{K \cdot 600n}{130n}$ where K represents width multiplier factor K=[1,5] in steps of 0.2 increments. The length of the device is kept constant. We show results for seven V_{GS} bias conditions, V_{GS}=[0, 0.2, 0.4, 0.6, 0.8, 1, 1.2]V. Figures 7.21–7.27 on pages 155–161 display analysis for each V_{GS} voltage. Each figure consists of three graphs which show:

- mean value of drain current, $\bar{\mu}(I_D)$ [μA],
- standard deviation, $\sigma(I_D)$ [μA],
- relative standard deviation with respect to the mean value, $\frac{\sigma(I_D)}{\bar{\mu}(I_D)} \cdot 100[\%]$.

Each graph includes five curves for five different V_{DS} values (*i.e.*, V_{DS} = 0.3, 0.5, 0.7, 0.9, 1.1 V). Each curve shown on any of these graphs is a result of 21000 simulations which have been performed through Monte Carlo statistical analysis.

By observing mean value curves (graphs a) and standard deviation curves (graphs b) on all Figures 7.21–7.27, we notice a strong linear dependence of the mean value and standard deviation on factor K. For example, in Figure 7.23, when K changes from 1 to 5, $\bar{\mu}(I_D)$ varies from 5 μA to 35 μA for V_{DS}=1.1 V or increases almost 7 times. Similar increase can be noticed for standard deviation on graph b) of the same figure. On the other hand, variation of relative standard deviation is significantly suppressed and hardly goes beyond 10%. For instance, in Figure 7.24, we see that the relative standard deviation decreases from 13.3% to 12.6% when K changes from 1 to 5.

The Monte Carlo simulation indicates a systematic and significant rise of mean value and standard deviation with increase of factor K, *i.e.*, from K=1 to K=5. This translates into a weak corresponding variation of relative standard deviation. This is also consistent with the previously observed results from Part A of the experiment.

7.6 Conclusion

For advanced device structures/architectures, statistical manufacturing process and dimensional variations will be a more significant barrier to achieving required specification, high-performance, and yield. While the absolute control of processes and alignment is improving, the percentage variation must not be allowed to increase as it may have a significant impact on the design and test.

It has been shown that, with a careful design methodology, it is possible to reduce MOSFET drain current variance to certain degree. Obviously, a length of the device is the most critical factor which affects sensitivity to process variation. Also, we conclude that there is no strong correlation between the width of the device and relative standard deviation. From designer perspective, in order to reduce the effect of process variations, one has to carefully weigh all factors which could contribute to the process variation uncertainty.

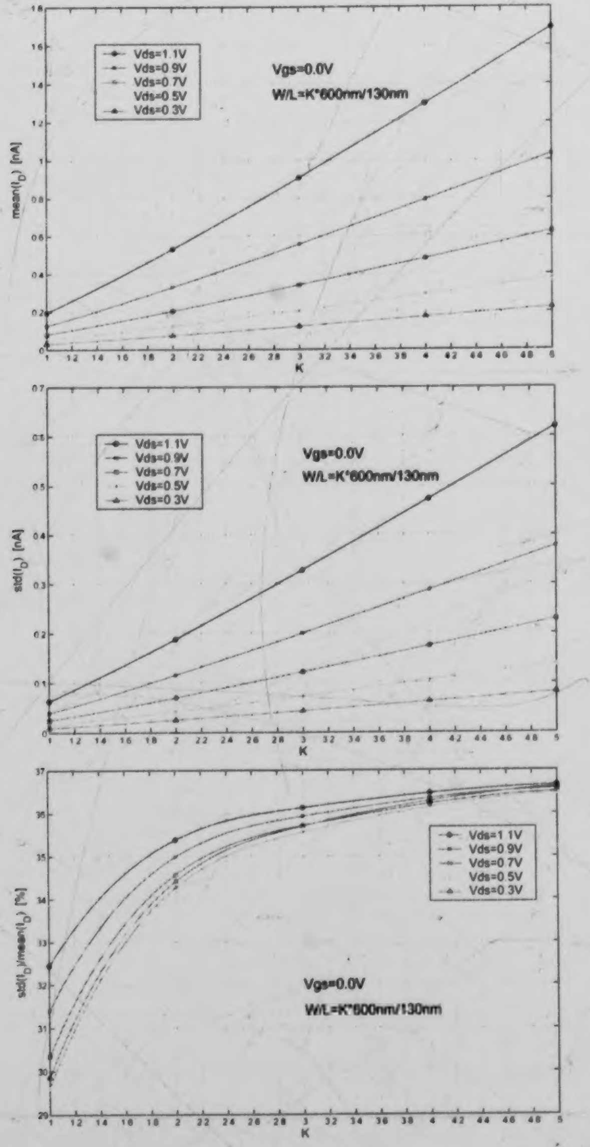

Figure 7.21: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=0 V and $\frac{W}{L} = \frac{K \cdot 600\ nm}{130\ nm}$

a) I_D mean: $\bar{\mu}(I_D)$ vs. K

b) I_D standard deviation: $\sigma(I_D)$ vs. K

c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

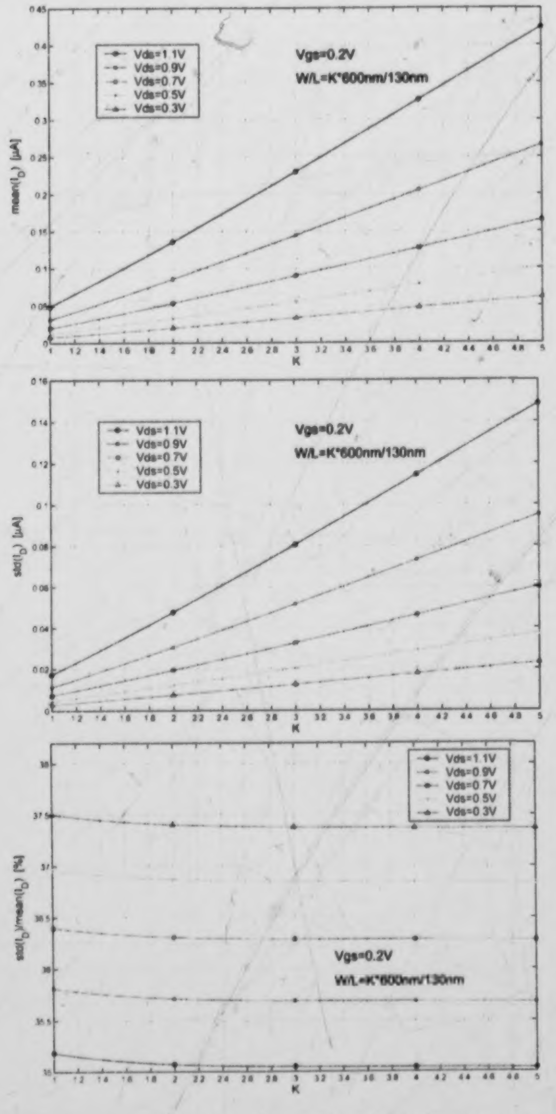

Figure 7.22: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=0.2 V and $\frac{W}{L} = \frac{K \cdot 600\ nm}{130\ nm}$

a) I_D mean: $\bar{\mu}(I_D)$ vs. K

b) I_D standard deviation: $\sigma(I_D)$ vs. K

c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

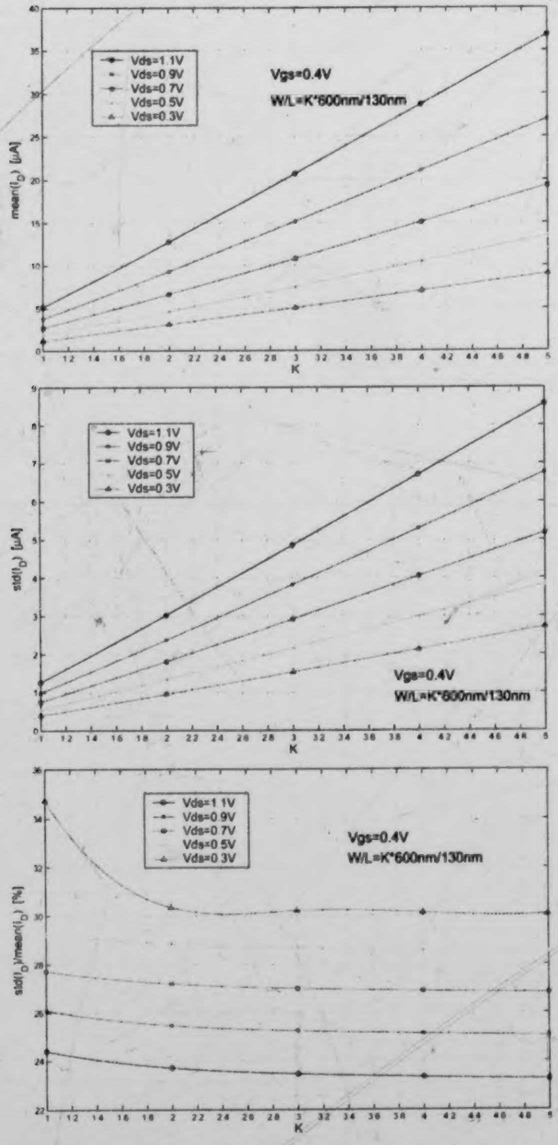

Figure 7.23: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=0.4 V and $\frac{W}{L} = \frac{K\cdot 600\ nm}{130\ nm}$
a) I_D mean: $\bar{\mu}(I_D)$ vs. K
b) I_D standard deviation: $\sigma(I_D)$ vs. K
c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

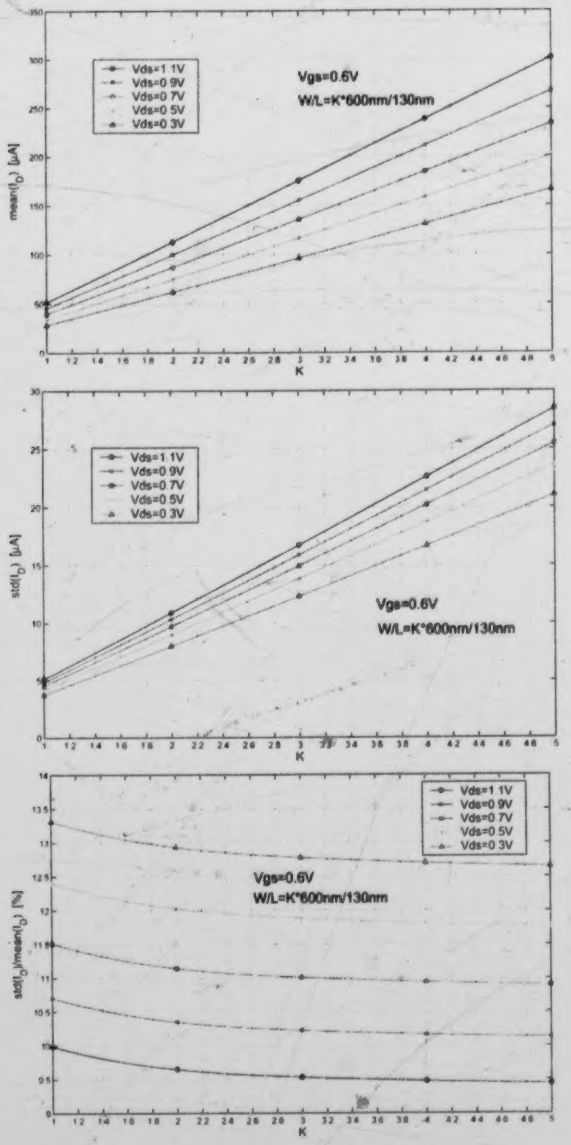

Figure 7.24: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=0.6 V and $\frac{W}{L} = \frac{K \cdot 600\ nm}{130\ nm}$

a) I_D mean: $\bar{\mu}(I_D)$ vs. K

b) I_D standard deviation: $\sigma(I_D)$ vs. K

c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

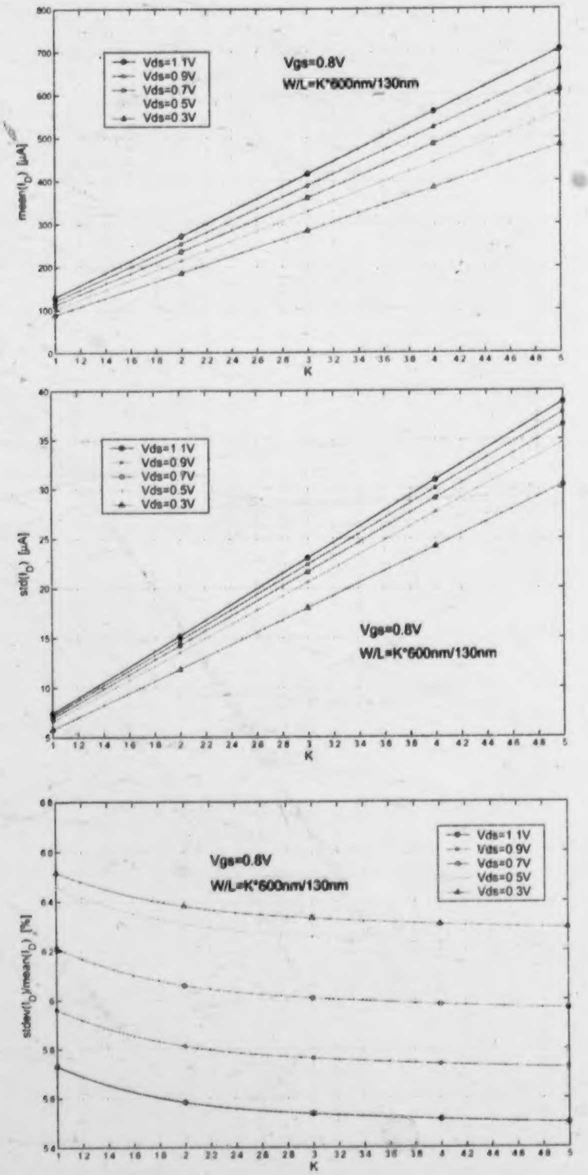

Figure 7.25: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=0.8 V and $\frac{W}{L} = \frac{K \cdot 600\ nm}{130\ nm}$

a) I_D mean: $\bar{\mu}(I_D)$ vs. K

b) I_D standard deviation: $\sigma(I_D)$ vs. K

c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

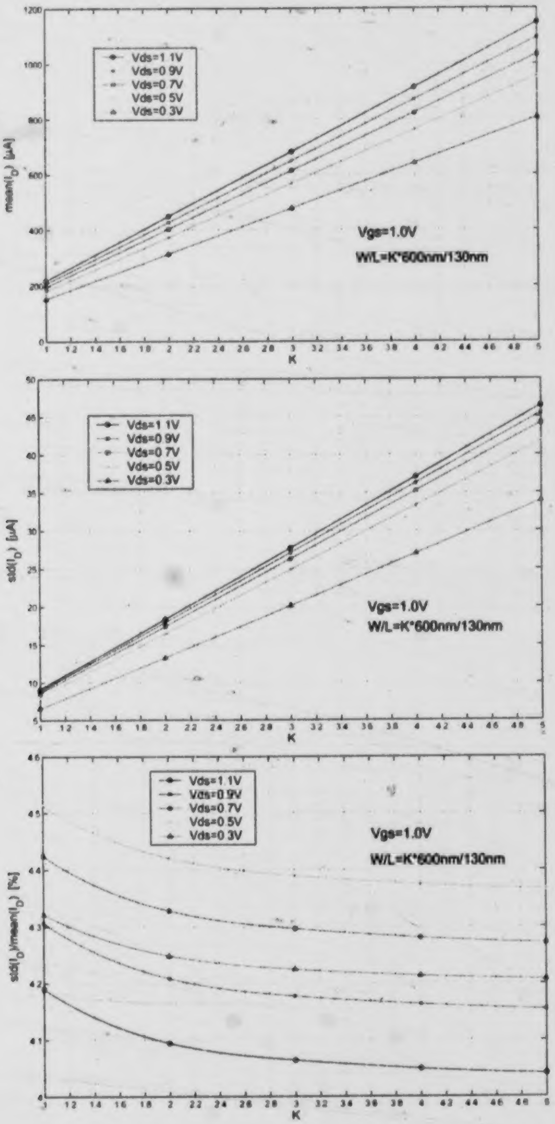

Figure 7.26: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=1.0 V and $\frac{W}{L} = \frac{K \cdot 600\ nm}{130\ nm}$

a) I_D mean: $\bar{\mu}(I_D)$ vs. K

b) I_D standard deviation: $\sigma(I_D)$ vs. K

c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

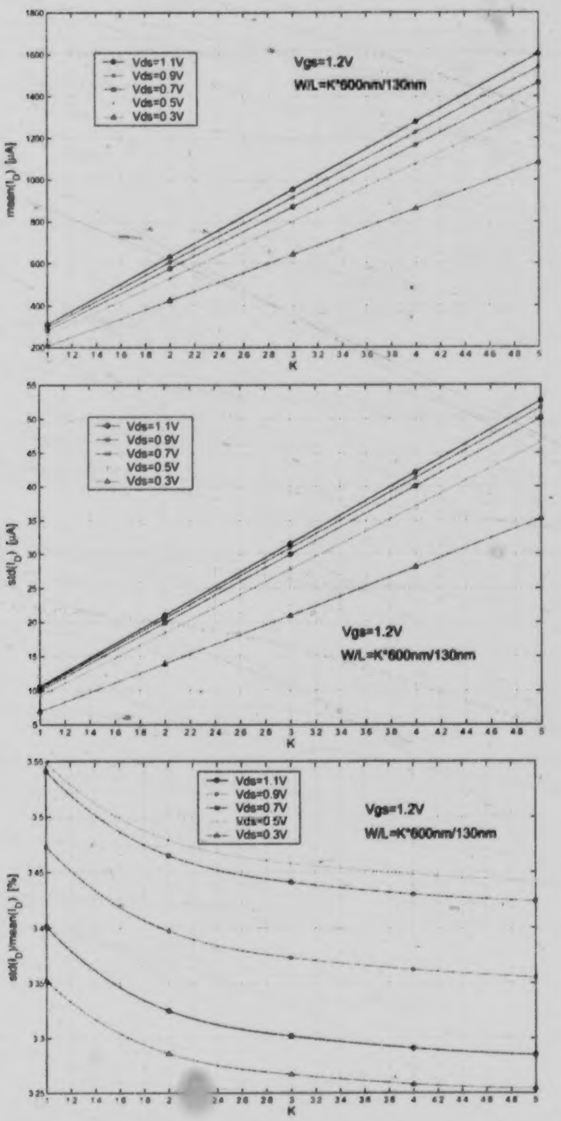

Figure 7.27: Drain current characterization of the MOSFET device with variable aspect ratio for V_{GS}=1.2 V and $\frac{W}{L} = \frac{K\cdot 600\ nm}{130\ nm}$
a) I_D mean: $\bar{\mu}(I_D)$ vs. K
b) I_D standard deviation: $\sigma(I_D)$ vs. K
c) I_D relative variation: $\frac{\sigma(I_D)}{\bar{\mu}(I_D)}$ vs. K

(no text)

Chapter 8

Analog Current Based Test for Resistive Fault Models

8.1 Introduction

Power supply current test methodology has been effectively used in testing of digital circuits for many years. It has been proven that the method itself offers a powerful tool for detection of various faults such as resistive short and bridging faults, which otherwise couldn't be screened by functional test [158], [56], [13]. The huge success in current monitoring for digital circuit has not produced similar results in testing of analog circuits. On the contrary, many attempts to apply similar approach to detect defects in analog circuits fail to produce strong and reliable alternative to the existing specification-based analog testing. Due to the nature of analog devices, application of power supply current testing to analog circuits has been a challenging task.

Analog circuits have complex relations between input and output signals. IC tests for analog circuits are generated directly from the circuit specifications, without reference to an analog fault model. With a large number of specifications, testing becomes exceedingly expensive and time consuming. An even more difficult situation occurs in testing of highly integrated analog devices. Today system-on-chip devices provide a level of integration far beyond traditional mixed-signal circuits. Observability and accessability of internal nodes is significantly reduced, and functional testing of analog devices in such environment is becoming very difficult

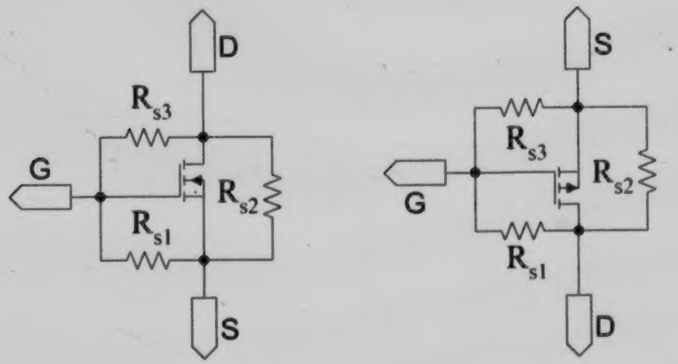

Figure 8.1: N-type and P-type MOSFET resistive short fault model

[27].

Effective early screening of defective chips could directly result in significant savings in the terms of test time and cost. We explored a potential advantage of the current-based test method for analog circuits to quickly screen defective dice, at the earliest stage during production test, before more comprehensive parametric/specification test is applied.

8.2 Current-Based Testing of Analog Circuits

In current monitoring test technique, power supply current drawn by the circuit under test is monitored and compared to the reference current value. It is assumed that a faulty circuit produces an abnormal or at least significantly different amount of current compared to the current produced by fault-free circuits. In a presence of a fault, the level and the shape of this current change, providing us with a tool to detect a faulty device.

A number of methods have been proposed in application of current-based test to analog circuits. Wang *et al.* used the spectrum of the power supply current to construct the statistical signature and detect a faulty circuit [213]. However, the analysis has been done for catastrophic bridging and open faults only. Similarly, Camplin *et al.* observed the correlation between changes of the power supply cur-

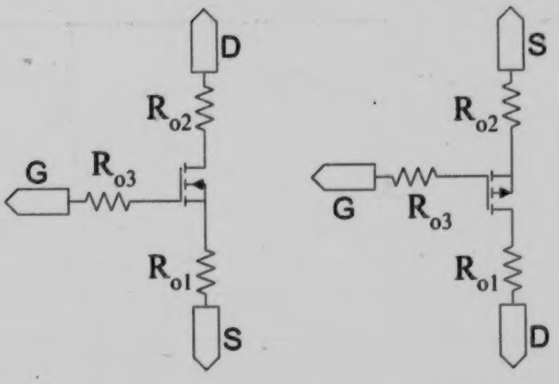

Figure 8.2: N-type and P-type MOSFET resistive open fault model

rent due to the catastrophic faults [19]. This fault analysis doesn't produce sufficient insight about potential of the proposed method without taking into account resistive short and conductive open defects. Lindermeir *et al.* considered more subtle parametric faults as well as manufacturing process and measurement noise in order to achieve more robust test design [101]. They chose trapezoid input signal rich in harmonics in order to better expose faults. In deeply embedded environment, precision of the on-chip generation of such input signal as well as limitation in detection of parametric faults [169] could reduce fault coverage. Noticeable drawbacks in some of the methods involve lack of consideration for process tolerances, which undoubtedly plays an important role in threshold setting and, as a result, impairs accurate fail/pass decision. I_{CCQ} method has been proposed by Lammeren [206]. Unfortunately, the author doesn't provide details about the type of defects detected by this method.

Resistive short and open faults present statistically far higher percentage of faults than catastrophic ones. Hard faults affect design's function quite noticeably, and, consequently, their detection is relatively easy process. Moreover, methods which require complex input signals generated in frequency and time domain for test detection could be questioned from the perspective of efficiency and accuracy. Generation as well as response evaluation precision of such signals has already been considered as a one of major obstacles for specification-based test in highly

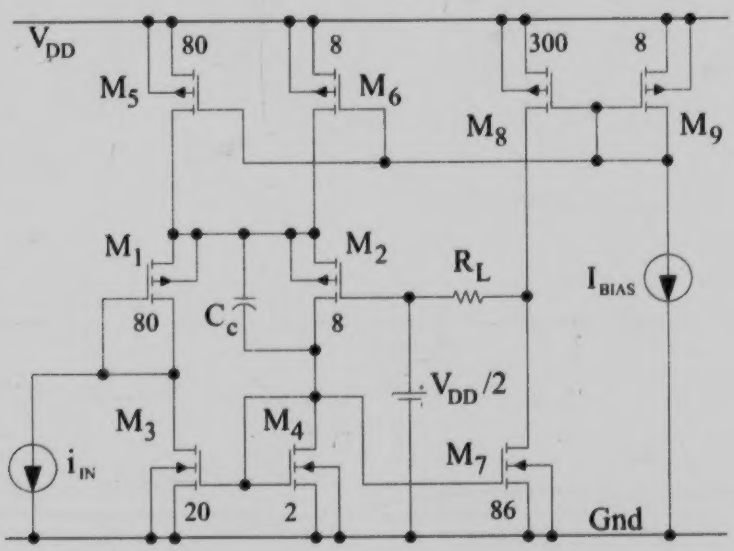

Figure 8.3: Circuit under test: current amplifying cell

integrated environments.

We extend fault detectability research to deep sub-micron 0.13 μm technology and investigate the power supply current method approach in testing of the typical analog circuit for resistive open and short set of faults. These kind of faults are caused by defects which manifest themselves as resistances seen between the gate, source and drain ports. Defect-oriented fault models shown in Figure 8.1 and Figure 8.2 assume defects within the gate of MOSFET transistors, but also to some degree represent metal interconnects and opens. More about defect-oriented faults could be found in [165]. We show that under certain circumstances, a presented two-step I_{DD} test approach with optimized DC input could be efficiently utilized as a complementary test technique. We show advantages, limitations, and scope of the current-based test for the tested type of analog circuits in 0.13 μm CMOS technology.

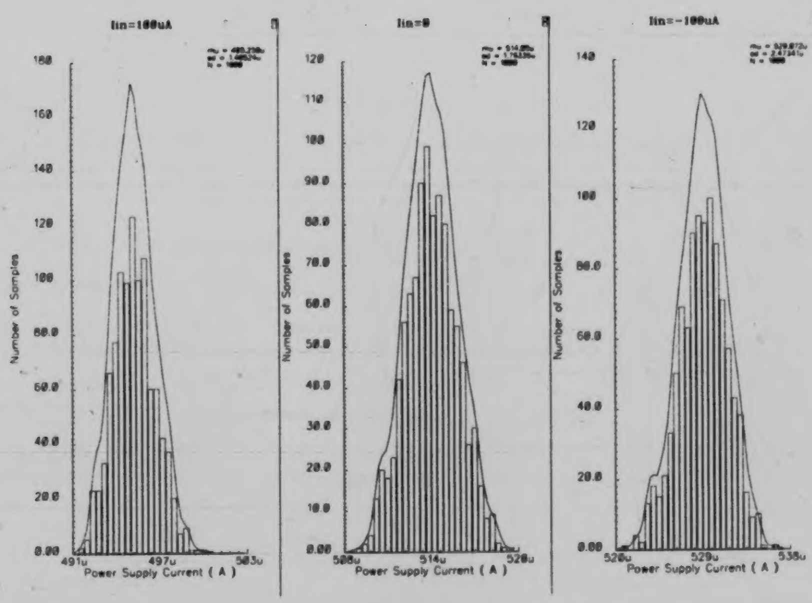

Figure 8.4: I_{DD} distribution of 1000 samples for three values of I_{IN}

8.3 Experimental Simulations

To evaluate feasibility of the proposed methodology, a simulation experiment was conducted with a sample layout of a typical analog circuit as a circuit under test. A voltage or current amplifier would be a circuit of choice as a most common analog circuit. For the purpose of more general conclusion, we decided to use a two-stage current amplifying cell with an asymmetric input stage. In that way, results from this experiment could be easily extended to similar, symmetric design such as standard two stage voltage amplifier. The tested circuit is designed in 0.13 μm standard CMOS process with 1.2 V power supply. A current amplifying cell circuit is shown in Figure 8.3.

Table 8.1: Process Parameters Standard Deviations

Parameter	BSIM3v3 Name	Standard Deviation σ
oxide thickness, NMOS	tox_n	0.5e-10 [m]
oxide thickness, PMOS	tox_p	0.5e-10 [m]
intrinsic threshold voltage, NMOS	vth0_n	0.01 [V]
intrinsic threshold voltage, PMOS	vth0_p	0.012 [V]
mobility	μ0	1.0e-3 [m^2/Vs]
width	W	1.0e-9 [m]
length	L	1.0e-9 [m]

Table 8.2: I_{DD} Standard Deviations for Different I_{IN}

I_{IN} Input DC Current [μA]	I_{DD} Mean Value [μA]	I_{DD} Standard Deviation [μA]
2000	511.479	1.305
1500	511.030	1.303
1000	510.006	1.297
500	508.164	1.286
200	506.198	1.270
100	495.256	1.405
0	514.050	1.763
-100	529.072	2.473
-200	534.834	3.728
-500	506.632	11.117
-1000	409.594	22.789
-1500	254.152	33.547
-2000	66.609	40.594

8.3.1 Power Supply Current Characterization

As a first step of our experiment, we perform Monte-Carlo simulation analysis of the current amplifying cell with intention to characterize circuit's I_{DD} current with respect to input DC stimuli and explore its variation limits in the case of the defect-free circuit.

The simulation is conducted for randomly generated small variation in circuit's component values (resistors, capacitors) as well as manufacturing process parameters. The temperature of the simulated circuits is kept constant at 300K. The list of varied parameters from BSIM3v3 model is shown in Table 8.1. Circuit's parameters are varied with 3σ standard deviation equivalent to 10% of element's nominal

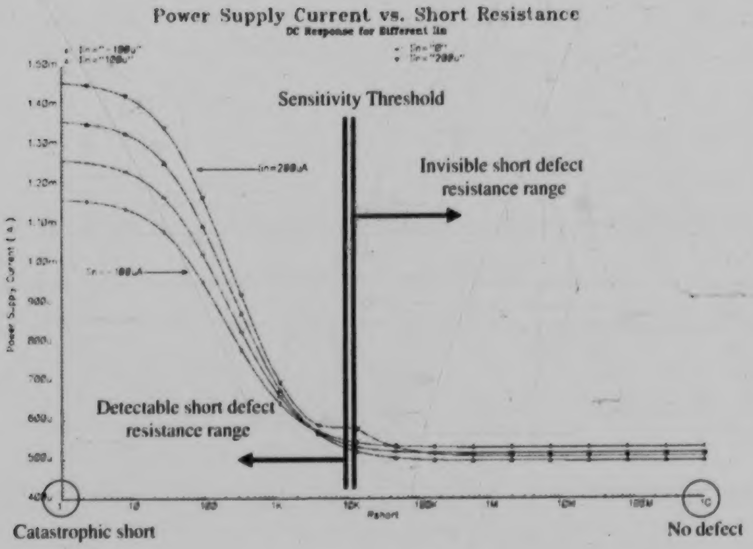

Figure 8.5: Power supply current vs. short defect resistance for different I_{IN}

values. All values are considered to follow Gaussian distribution. We examined correlation between standard deviation of the power supply current and input DC stimuli. Characterization of I_{DD} for each I_{IN} DC value is simulated on 1000 circuit samples. A part of the results could be seen in Figure 8.4. Standard deviation of I_{DD} changes form 1.4 μA for I_{IN}=100 μA to 2.47 μA for I_{IN}=-100 μA. Apparently from Figure 8.4, expected defect-free variation of I_{DD} is a function of the input signal. This analysis provides insight about the range of input currents for which minimum standard deviation of circuit's defect-free power supply current occurs. In other words, we determine a value of input currents for which potential defects are most visible in I_{DD} and least masked by the defect-free I_{DD} variations.

In a presence of defect, additional power supply current which falls within the set boundary of I_{DD} cannot be distinguished from the fault-free current. Therefore, the objective is to minimize variation in I_{DD} due to the process tolerances, and to

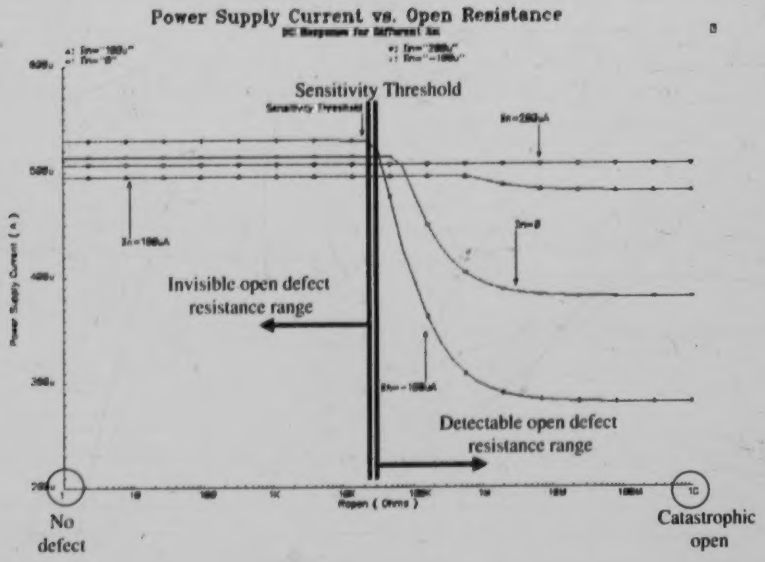

Figure 8.6: Power supply current vs. open defect resistance for different I_{IN}

maximize variation in I_{DD} due to the introduced defects.

In our experiment, we observed standard deviations of I_{DD} for input current range I_{IN}=[-2 mA,2 mA]. Based on the results shown in Table 8.2, I_{DD} standard deviation increases significantly for $I_{IN} \leq$-100 μA. For such input signals, expected variations of the fault-free power supply current mask defective currents and obstruct effective fault screening. Therefore, we decided to investigate behavior of each introduced fault for I_{IN}=[-100 μA, 1 mA] and to optimize it for the maximum variation in I_{DD}.

8.3.2 Fault Coverage

All faults were separated into two groups: resistive opens and resistive shorts. They have been observed at the transistor level. In our experiment, we used defect-oriented resistive fault models shown in Figure 8.1 and Figure 8.2. The complete set

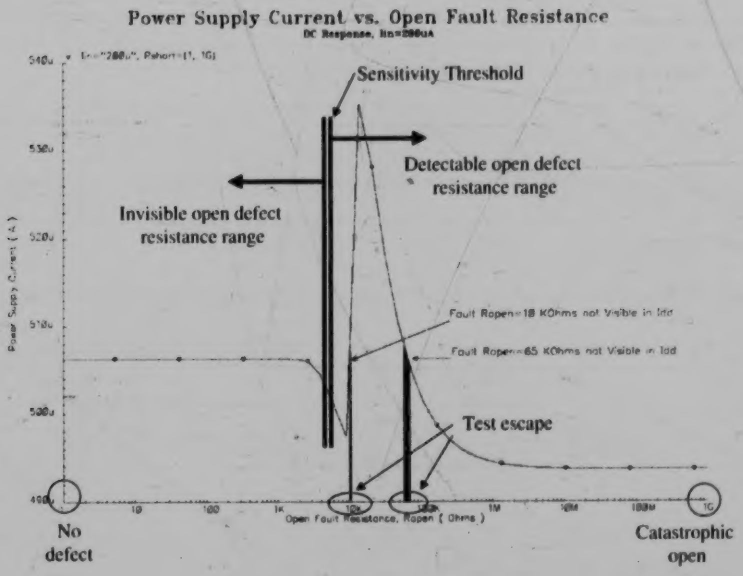

Figure 8.7: Invisible resistive open defects of 10 kΩ and 65 kΩ

of all possible resistive bridging faults to be considered is relatively large even for circuits with small number of gates. However, location of the points in the circuit which are likely to be connected through the bridging defect is layout-dependant. Therefore, we restricted our study to those faults between the gate, source, and drain of the MOSFET device.

Although the fault coverage term is not defined for fault models with the infinite number of faults (*i.e.*, infinite number of fault resistive values) that we utilized in this experiment, we are using this term to describe the efficiency of the proposed method in terms of detectability of the minimum resistive open fault and maximum resistive short fault. Therefore, we introduce the term sensitivity threshold (ST). ST for open fault is minimum detectable resistive open. For shorts, we define ST as a maximum detectable resistive short. ST can be set arbitrarily based on the I_{DD} standard deviation. In our study, sensitivity threshold marks a value of the

Table 8.3: I_{DD} Variation for Short Defects in Transistors M_1–M_6

Transistor	**Short**	**ΔI_{DD} [μA]**	**I_{IN} [μA]**	**ST [Ω]**
M_1	R_{S1}	N/A	N/A	N/A
M_1	R_{S2}	10.45	200	220k
M_1	R_{S3}	10.45	200	220k
M_2	R_{S1}	61.28	100	8M
M_2	R_{S2}	25.41	100	15M
M_2	R_{S3}	35.52	0	800k
M_3	R_{S1}	165.34	-100	4M
M_3	R_{S2}	35.37	-100	1.5M
M_3	R_{S3}	5.13	0	600k
M_4	R_{S1}	165.34	-100	10M
M_4	R_{S2}	165.34	-100	10M
M_4	R_{S3}	N/A	N/A	N/A
M_5	R_{S1}	550.28	500	20M
M_5	R_{S2}	1256.41	500	2M
M_5	R_{S3}	504.12	0	250M
M_6	R_{S1}	550.28	500	20M
M_6	R_{S2}	1256.71	500	2M
M_6	R_{S3}	504.12	0	250M

fault resistance when power supply current changes in value more than its standard deviation.

To be detectable, faulty current of the circuit under test has to be distinguishable from the normal variations of I_{DD} current. Since the fault-free leakage current is a function of many variables values of which have high variations and uncertainty, the faulty current can be either masked with them, or wrongly reported in the case of an inappropriately set threshold level. The threshold level has to be set accordingly so it takes into account state dependent variations of the leakage current, process variations, and temperature.

We introduced single faults into the testing circuit and explored variation of

Table 8.4: I_{DD} Variation for Short Defects in Transistors M_7–M_9

Transistor	Short	ΔI_{DD} [μA]	I_{IN} [μA]	ST [Ω]
M_7	R_{S1}	165.34	-100	12M
M_7	R_{S2}	56.24	100	1M
M_7	R_{S3}	31.07	200	5M
M_8	R_{S1}	876.23	0	30M
M_8	R_{S2}	990.21	-100	10M
M_8	R_{S3}	504.11	0	30M
M_9	R_{S1}	N/A	N/A	N/A
M_9	R_{S2}	504.11	0	30M
M_9	R_{S3}	504.11	0	30M

I_{DD} for the set of input currents within the range previously determined during I_{DD} characterization. The resistance of each fault was varied from 0 Ω to 1G Ω. According to study in [158], vast majority of bridging shorts have resistance of less than 20 kΩ. We show in Table 8.3 and Table 8.4 that ST for all faults is at least ten times higher, which implies high level of detectability.

In Figure 8.5, we show I_{DD} vs. R_S characteristics for introduced R_{S2} fault in transistor M_5 of the circuit under test. It can be seen that when changing resistance of the resistive short fault, the maximum variation of the power supply current is observed for I_{IN}=200 μA. In other words, defect will be most observable if this current is applied at the input. Similarly, samples of I_{DD} vs. R_O characteristics are shown in Figure 8.6 for R_{O2} open fault introduced in transistor M_2. Here, it is obvious that I_{IN}=-100 μA makes the fault most visible and detectable.

Throughout our experiment, we confirmed that all short faults shown in Figure 8.1 have been detected. Indeed, appropriate input signals to the circuit had to be supplied in order to make a fault visible. Some faults resulted in significant change of supply current, while the others produced smaller but still detectable variations. Table 8.3 and Table 8.4 lists I_{DD} variations, STs, and corresponding input signals for all short resistive faults. The detection rate of open resistive faults, depicted in

Table 8.5: I_{DD} Variation for Open Defects in Transistors M_1–M_9

Transistor	Open Defect	ΔI_{DD} [μA]	I_{IN} [μA]	ST [Ω]
M_1	R_{O1}	40.12	100	6k
M_1	R_{O2}	40.17	100	4k
M_2	R_{O1}	248.28	-100	20k
M_2	R_{O2}	248.28	-100	200
M_3	R_{O1}	117.67	-100	50
M_3	R_{O2}	117.52	-100	2k
M_4	R_{O1}	13.40	0	600
M_4	R_{O2}	13.11	0	30k
M_5	R_{O1}	119.88	0	150
M_5	R_{O2}	119.67	0	10
M_6	R_{O1}	11.60	100	15k
M_6	R_{O2}	11.50	100	300
M_7	R_{O1}	42.90	-100	5
M_7	R_{O2}	43.30	-100	100
M_8	R_{O1}	396.61	0	100
M_8	R_{O2}	395.12	0	5
M_9	R_{O1}	3358.25	0	20k
M_9	R_{O2}	3351.93	0	500

Figure 8.2, was 67%. All R_{O3} open faults in the gate of transistors were practically invisible by this test approach. This was expected since the MOSFET gate is already isolated and conducts no current. An ohmic open defect in the MOSFET gate with sufficiently high resistance (modeled by R_{O3}) causes so called *floating gate* effect[1]. This fault inevitably affect the shape of circuit's transient and AC characteristic, and could be screened by specification based test. Table 8.5 lists I_{DD} variations, STs, and corresponding input signals for all open resistive faults. Variation in power supply current ranges from 13 μA for transistor M_4 to more then 3 mA

for transistor M_9. For some open faults I_{DD} vs. R_O characteristic have an irregular shape. Although with resistance above sensitivity threshold, these resistive open faults may produce same level of I_{DD} current as a fault-free circuit, which makes them theoretically invisible for this test. This is shown in Figure 8.7 for R_{O1} introduced in transistor M_1. Resistive opens R_{O1}=10 kΩ and R_{O1}=65 kΩ will set a level of power supply current to the same level as in fault-free circuit. Nevertheless, the slope in the vicinity of these points is very high, which narrows the band of such faults invisible for this test and, statistically, limits their occurrence to the marginal level.

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[1] A floating gate defect occurs in a circuit when the gate of transistor becomes disconnected from its controlling input and loses its ohmic electrical connection with the rest of the circuit.

8.4 Conclusion

A non-specification based test approach for analog circuits in deep sub-micron 0.13 μm CMOS process has been explored. The method is based on power supply current measurements and is intended as a complementary test suite for early fault detection. The method targets non-catastrophic resistive open and short faults within the gate of MOSFET devices. Since no complex input signals are required for fault excitation, it can be a complementary test approach to existing DC, AC, and transient specification oriented test. With certain constrains, 100% of short faults and 67% of open faults have been detected.

(no text)

Chapter 9

Summary and Conclusions

This thesis presented a focused effort to investigate the potentials of current-based test methodologies and offered possible solutions in advanced technology processes. Such environments are characterized by the multitude of leakage effects and defect types which significantly challenge the effectiveness and capabilities of the present current test methodologies. A comprehensive study with emphasis on issues, requirements, and solutions for embedded current-based test in deep sub-micron environments was presented.

A built-in current monitoring solution has been identified as a way to address the challenges by enabling easier access to embedded cores. In the process of developing a sensor device topology, we outlined a set of requirements for the successful application of embedded monitors. A detailed analog behavior analysis of the proposed sensing device has been provided, and the sensor was evaluated in a current monitoring testing scheme. Furthermore, the effect of process variations on device's current was investigated, and a methodology for non-specification current test of analog circuits was proposed.

9.1 Thesis Summary

In Chapter 2, we provided basic background information, terminology, and definitions needed for better understanding of the work proposed in this thesis. We introduced the fundamentals of IC testing describing the test environments and concepts behind conventional IC testing including test objectives, stages, types, and methodologies.

Chapter 3 focused on the current test methodology for integrated circuits. The evolution of this type of test was presented along with elementary concepts behind it. We also described the present state-of-the-art scientific findings related to mechanisms behind CMOS leakage currents in sub-micron technology processes. Understanding the leakage properties of deep sub-micron transistors is, beside design and performance related issues, also essential to guide effective solutions for current-based testing.

Chapter 4 elaborated on concepts and applications of power supply current monitoring. We outlined the requirements for the current monitor designs, and presented different techniques for current sensing. We also explored existing methodologies and summarized different design concepts and principles of current sensing in test applications. A comprehensive survey of the relevant current monitor devices reported in the literature was provided in this chapter.

Chapter 5 presented a novel topology of the embedded current amplifying device. We described a design and implementation of the novel built-in amplifier topology developed as a front-end device of a built-in monitoring system (*i.e.*, sensing and detection device).

Chapter 6 investigated the feasibility, scope, and limitations of the current test technique for digital circuits based on the proposed built-in current sensing device. The novel sensor topology was successfully employed in a current monitoring testing scheme. For verification purposes, the sensor's performance was evaluated on several types of digital circuits.

Chapter 7 provided insight into the effects of process variations on the drain current of a MOSFET device. A comprehensive characterization of the drain current showing the scope of the variability due to the process variation was also provided. The results indicated that circuit design techniques could minimize, to some degree, rising process uncertainties and complement more advanced process techniques that reduce variability.

Chapter 8 explored a novel non-specification based test approach for analog circuits in a deep sub-micron CMOS process. The proposed test method is based on power supply current measurements and is intended to be a simple complementary tool of the comprehensive test suite for early fault detection. The method targets non-catastrophic resistive open and short faults which may occur within a MOSFET device.

9.2 Recommendations for Further Studies

There are plenty of opportunities for the extension of the work presented in this thesis, and some initiatives are already under way. We outline the recommendations for future research that may further advance the knowledge in this area.

9.2.1 Circuit Topology Development and Improvement

It has been shown that the built-in test approach may solve some disadvantages of external test equipment, most importantly, processing speed and easier access to embedded cores. The question arises - how much can we rely on built-in devices when making decisions which could have a profound effect on the test economics? The answer to this question requires a careful evaluation of the reliability, stability, and accuracy of the given sensor topology. Further research is needed to develop the tools and/or methodology to verify the correctness of the sensing and monitoring device itself. In this sense, development of the supporting A/D and/or digital circuitry may be an appropriate way to address this issue.

Further improvements in the domain of circuit topology are undoubtedly possible. A research group at the Rochester Institute of Technology extended the work on the development of the presented current sensor device and showed that the process variation effects on sensor's performance could be minimized by introducing a simple feedback in the sensor amplifier. It is expected that the details of their work be published in IEEE Transactions on VLSI Systems. Yet, at the time of submission of this thesis, the particular reference is not yet finalized.

Moreover, refinements could be envisioned by designing amplifying stages with enhanced performance and decreased sensitivity to environmental and process parameter changes. Several alternatives for topology optimization with self-calibrating mechanisms were also conceived during the course of this work, and some of the ideas are presently in the implementation phase. In particular, a sensor using a differential approach has been fabricated with a temperature-compensated input stage to reduce the environmental influence.

9.2.2 Test Methodology Development and Application

While a sizeable part of the work in this thesis is dedicated to the development of the sensor topology suitable for built-in test applications, it is definitely worth mentioning that continuing exploration of current-based test methodologies requires further attention. Consideration may be given to the development of novel signature analysis techniques to reduce or eliminate the need for physical failure analysis. Statistical methods could be an alternative to detect a failing die of a particular class to reliably pre-select and prioritize input to physical failure analysis.

Extensions to the existing current techniques may prove adequate for the next several technology nodes, but further research in the development of new methodologies is required. An idea would be to develop novel current test methods which could identify the root causes for failure based on test information without resorting to physical failure analysis. A key enabling technology is a characterization test method capable of distinguishing individual defect types. Integration of electrical characterization data with layout data and test results may also offer capabilities for improved test methodologies.

It is clear that adequate analog DFT and BIST techniques should be explored further. No equally effective alternative to specification-based analog testing exists and more research in this area is needed. Analog BIST could be suggested as a possible solution and area for more research. Fundamental research can be extended to identify techniques that enable reduction of test instrument complexity or the elimination of the need for external instrumentation.

9.2.3 Process Variation Analysis

We showed the degree to which variations in the process parameters may affect the current of the MOSFET device. In the development of any current test techniques, process variation analysis should be taken into account. Several ideas for further research could be identified in this domain. In the application of current-based test to analog circuits, it might be worth exploring if it is possible to develop a model of circuit's supply current which would incorporate currents of circuit's individual branches with a total standard deviation as a function of standard deviations of each branch. Understandably so, such an approach would make sense for analog circuits only as they contain relatively few number of branches and devices.

Statistical modeling may be a tool to develop a failure analysis method for analog circuits which could be automated. Such a model may be used to predict more accurately the total expected process variation and it would clearly reveal the maximum resolution of any current-based test. This statistical method for determining the standard deviation of the power supply current could be correlated with other parameters to yield a more effective tool for not only fault detection, but also the characterization of analog circuits.

9.3 Concluding Remarks

The evolution of the IC process technology will inevitably dictate the trends in the current-based test domain. As it stands now, IC test methods are becoming more complex, less effective, and with constantly reducing resolution. The likelihood that a single comprehensive test solution will emerge seems quite remote. Instead, we believe that the future successful test methodology must rely on a variety of test techniques each of which will target a particular segment of defects. The emphasized need for multi-test solutions will become even more apparent in the multi-domain and heterogenous micro-systems in which the increasing variety of possible defects will exist far beyond the reach of any single test approach.

In this context, current-based test will continue to play an important role in addressing the segment of defects inherently present in today's CMOS circuits. As such, it is expected to remain in a typical test portfolio for the next 4-5 technology nodes. The significant scientific efforts to reduce leakage currents in CMOS circuits are driven primarily by the consumer market and the need for ultra low-power devices. Advancements in technology processes coupled with other techniques may also alleviate to some degree the present challenges for current-based test and extend its use. The struggle to keep CMOS topology effective will ultimately determine the fate of today's current-based test. Indeed, the application of current-based test will evolve with the technology, but its basic concept may, eventually, outlast the CMOS circuit architecture.

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